Semiconductor Corporation

CS8905

Programmable Music Processor

Features

- Polyphonic up to 16 notes
- Multi-timbral up to 16 simultaneous timbres
- Oscillator frequencies to 48 MHz (46.875 kHz sampling rate)
- Stereo 16 bit digital audio output
- On-chip 256x15 Algorithm RAM, and 256x19 Parameter RAM
- Built-in sine and ramp data
- Addresses up to 1Mx12 sample ROM directly, 64Mx12 using paging
- Single +5V supply CMOS, 50 mW typical power dissipation
- 68 pin PLCC package

General Description

The CS8905 is a high performance programmable signal processor which is specially designed for music and sound generation applications such as music synthesis and digital effects processing. This device features 19-bit internal data paths, a 19-bit two's complement adder, a 12 x 12 two's complement multiplier, two 24-bit accumulators and a 32-bit output shift register. As a music synthesizer, the CS8905 is capable of generating 16 notes of polyphony with a high quality 16-bit stereo digital audio output at a 44.1 kHz sampling rate. For wave table synthesis applications, up to 64 Msamples of external sample memory may be addressed, and the CS8905 can generate linear envelope segments under external microprocessor control. The micro-programmable architecture of the CS8905 also makes this device well suited for use as a digital effects processing engine.

ORDERING INFORMATION

CS8905-CL 68-pin PLCC

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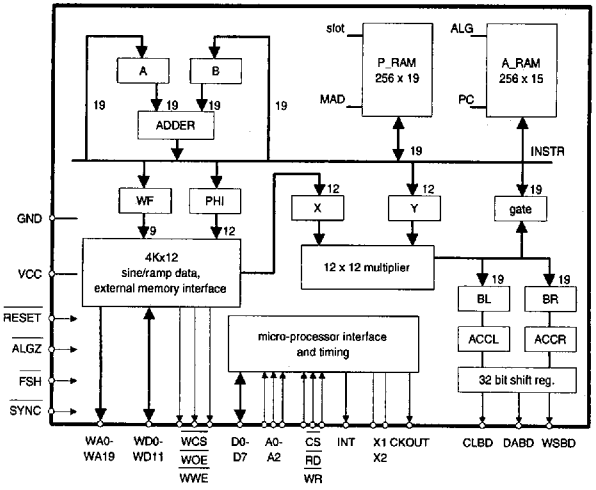

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature (Power Applied)	T_A	-40	-	+85	°C
Storage Temperature	-	-65	-	+150	°C
Voltage on any Pin	-	-0.5	-	V_{CC}+0.5	V
Supply Voltage	V_{CC}	-0.5	-	6.5	V
Maximum I_{OL} per I/O Pin	-	-	-	10	mA

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.75	-	5.25	V
Operating Ambient Temperature	T_A	0	-	70	°C

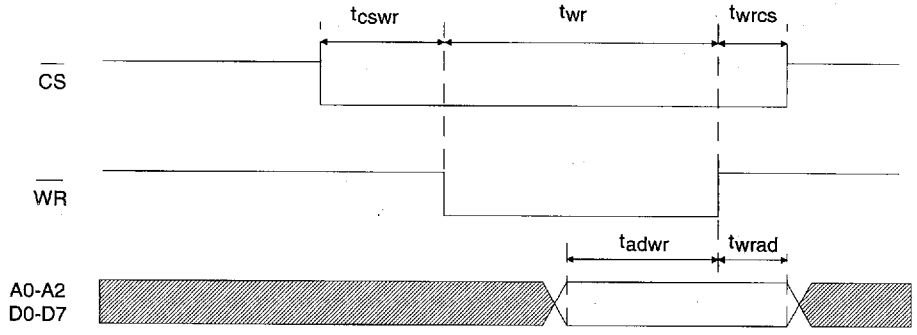
D.C. CHARACTERISTICS (T_A=25°C, V_{CC}=5V±5%)

Parameter	Symbol	Min	Typ	Max	Units
Low-Level Input Voltage	V_{IL}	-0.5	-	0.8	V
High-Level Input Voltage	V_{IH}	2.0	-	V_{CC}+0.5	V
Low-Level Output Voltage at I_{OL}=3.2 mA	V_{OL}	-	-	0.45	V
High-Level Output Voltage at I_{OH}=-0.8 mA	V_{OH}	2.4	-	-	V
Power Supply Current at Oscillator Frequency=45.1584 MHz (Note 1)	I_{CC}	-	10	25	mA

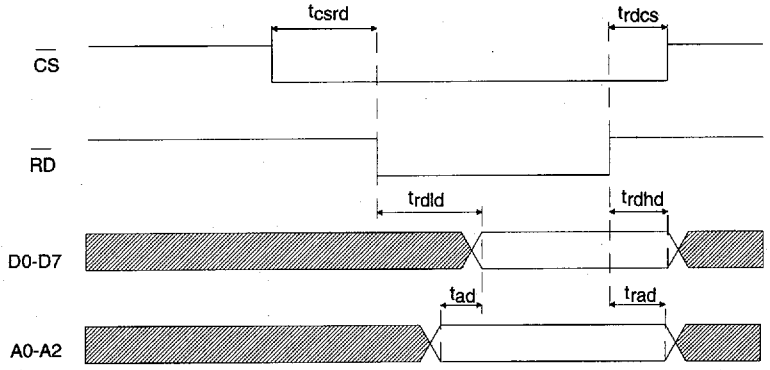
Notes: 1. Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, Power Supply Current does not include output loading

A.C. CHARACTERISTICS (T_A=25°C, V_{CC}=5V±5%, Digital Inputs at Logic "1"=Vcc; Logic "0"=DGND, load capacitance=80pF for all outputs except X2)

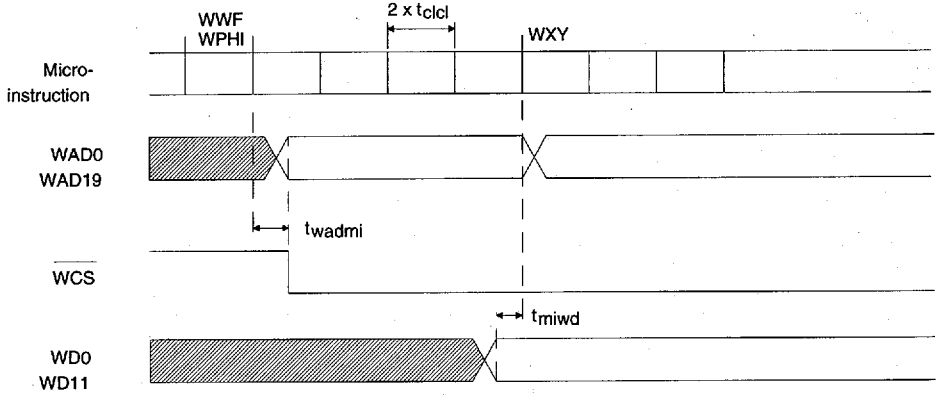
Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency	1/tclcl	0	45.1584	48	MHz
$\overline{CS}$ Low to $\overline{WR}$ Low	tcswr	50	-	-	ns
$\overline{WR}$ High to $\overline{CS}$ High	twrcs	20	-	-	ns
A0-A2, D0-D7 Valid to Rising $\overline{WR}$	tadwr	20	-	-	ns
A0-A2, D0-D7 Valid After Rising $\overline{WR}$	twrad	10	-	-	ns
$\overline{WR}$ Pulse Width	twr	50	-	-	ns
$\overline{CS}$ Low to $\overline{RD}$ Low	tcsrd	50	-	-	ns
$\overline{RD}$ High to $\overline{CS}$ High	trdcs	20	-	-	ns
$\overline{RD}$ Active to Valid Data Out	trdld	-	-	50	ns
Data Out Hold From $\overline{RD}$	trdhd	10	-	-	ns
A0-A2 Valid to Valid Data Out	tad	-	-	50	ns
A0-A2 Hold From $\overline{RD}$	trda	10	-	-	ns
Recover From Control Write	trecover	32xtclcl+10	-	-	ns
CLBD Period	tclbd	-	32xtclcl	-	-
WAD0-19 Valid From WWF or WPHI Micro-Instruction	twadmi	-	-	10	ns
WD0-11 Valid Before WXY Micro-Instruction	tmiwd	10	-	-	ns
$\overline{WOE}$ High From RSP ClearB Micro-Instruction	twoemi	-	-	10	ns
WD0-11 Out Valid (Y Register) From $\overline{WOE}$ High	twoewd	-	tclcl	-	ns
$\overline{WWE}$ Low From $\overline{WOE}$ High	twoewe	-	2 x tclcl	-	ns
$\overline{WWE}$ High to WD0-11 High Z	twewd	-	tclcl	-	ns
$\overline{WWE}$ High to $\overline{WOE}$ Low	twewoe	-	tclcl	-	ns



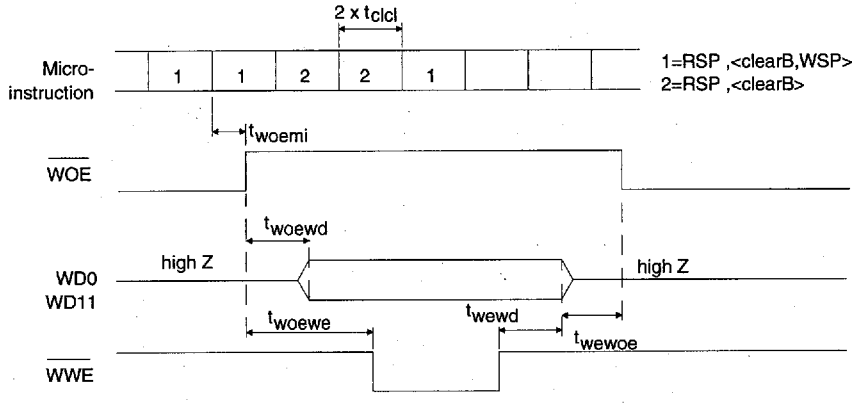
Microprocessor Write to CS8905



Microprocessor Read from CS8905



Sample Memory Read



Sample Memory Write

FUNCTIONAL DESCRIPTION

The CS8905 is a specialized high speed programmable signal processor for music and sound generation applications. The CS8905 signal processing unit includes a 19-bit two's complement adder, a 12 x 12 two's complement multiplier, two 24-bit accumulators and a 32-bit output shift register. The devices' internal data paths are 19 bits wide. Typical connections for a CS8905-based MIDI music synthesizer are indicated in Figure 1.

The CS8905 operates at one of two possible sampling rates. In the normal operating mode, the sampling rate is equal to the crystal oscillator frequency divided by 1024. In the "slow" mode, the sampling rate is the oscillator rate divided by 2048. The sample period, or synthesis frame, is divided into 16 time slots, which are referred to as synthesis slots. A sound generation algorithm for the CS8905 consists of 32 microinstructions, and one algorithm is executed during each synthesis slot.

An on-chip 256 x 15 Algorithm RAM (A-RAM) holds eight different synthesis algorithms [4 algorithms in slow mode]. A 256 x 19 Parameter RAM (P-RAM) provides 16 words of parameter data storage for each synthesis slot. The sound generation functions of the CS8905 are controlled by an external microprocessor which has access to the Algorithm RAM and the Parameter RAM. The Parameter RAM block for each synthesis slot provides a means for the external microprocessor to control the parameters of the synthesis algorithm used by the slot, and this

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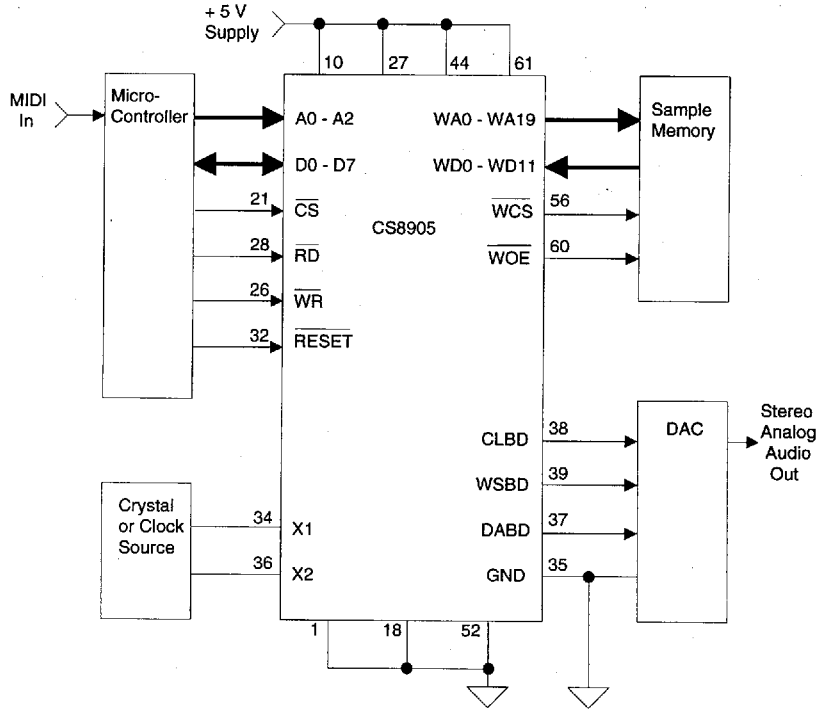


Figure 1. Typical Connection Diagram

memory block also provides working memory for the synthesis algorithm. The external microprocessor may write to either the A-RAM or the P-RAM during operation.

For music synthesis applications, each time slot is independent of the other slots, and each time slot may be used to generate one sound or note. During each slot time, one synthesis algorithm is executed and the output sample data from that algorithm is written to the left and right channel 24-bit accumulators. The signal processing unit controls the level and balance of the output from the slot by scaling the sample output to the accumulators under the control of the output mix parameters specified in the P-RAM block for that slot. The accumulators are specially designed to prevent digital overflow. At the end of each frame, the contents of the accumulators are transferred to the 32-bit output shift register and the accumulators are cleared. The shift register clocks the resulting sample data out serially to the external Digital-to-Analog Converter (DAC).

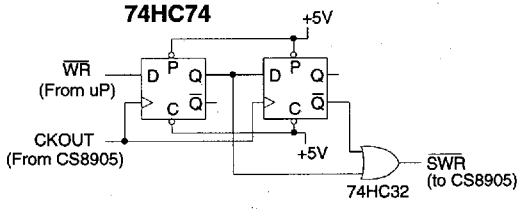
For other signal processing applications, such as generation of digital reverberation and chorus effects for musical applications, the 16 time slots available during each sample period may be used to run subroutines of a larger algorithm. In this case, parameters may be passed between time slots through the A register of the adder circuit, through the multiplier, or through external RAM.

The CS8905 can directly address up to 1 M x 12 of external memory. For high quality sampling algorithm implementations, paging techniques may be utilized to allow the CS8905 to address up to 64 Msamples of external sample memory. Sine wave and ramp data is built into the chip. The CS8905 is capable of generating linear envelope segments with a specified slope to allow creation of piecewise linear amplitude envelopes under external microprocessor control.

Microprocessor Interface

An external microprocessor controls the CS8905 synthesis functions by accessing the CS8905 Control Register, Interrupt Register, Algorithm RAM (A-RAM), and Parameter RAM (P-RAM). The Microprocessor electrical interface is a standard bus interface, comprised of the address lines A0-A2, the data lines D0-D7, the Chip Select signal $\overline{CS}$, the Write signal $\overline{WR}$, and the Read signal $\overline{RD}$.

If the external microprocessor timing and the CS8905 timing are asynchronous, then an external write synchronization circuit, such as that shown in Figure 2, should be employed to synchronize the $\overline{WR}$ signal from the external



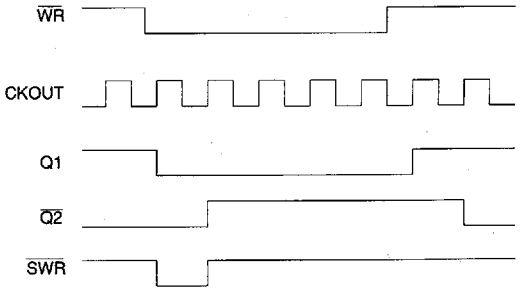


Figure 2. Write Synchronization Circuit

microprocessor with the CS8905 timing. This circuit assumes that data from the microprocessor is valid on the leading edge of $\overline{WR}$, and that the CKOUT period is shorter than the pulse width of $\overline{WR}$. If the external microprocessor timing and the CS8905 timing are derived from the same oscillator source, then the write synchronization circuit is not necessary.

The 256 x 15 Algorithm Ram (A-RAM) is organized as either 8 blocks of 32 words, or 4 blocks of 64 words in slow mode. Each word contains one micro-instruction, and each block of 32 instructions [64 in slow mode] makes up one algorithm. The last two locations in each block are reserved for microprocessor access and algorithm changes. Thus an algorithm consists of 30 micro-instructions [62 in slow mode] for sound generation. Internally, the CS8905 operates on a Master Clock, with a frequency equal to the crystal oscillator frequency divided by two. Each micro-instruction is executed in one cycle of the Master Clock.

The 256 x 19 bit Parameter RAM (P-RAM) is organized as 16 blocks of 16 words each. There is one 16 word x 19 bit block of P-RAM associated with each synthesis slot. The 16 word block of P-RAM associated with a particular synthesis slot is used to specify the synthesis algorithm number and the associated parameter data to be used for that synthesis slot. The P-RAM also functions as working RAM for the synthesis algorithm computations. The parameter types, parameter data formats and parameter addresses required for that slot depend on the specific synthesis algorithm being utilized for the slot. However, parameter location 15 in each 16-parameter block utilizes a common format which specifies the algorithm to be used for the slot. Location 15 also contains the Idle bit (I) which is used to force the associated synthesis slot to an idle mode, and the Interrupt Mask bit (M) which is used to enable/disable the generation of interrupts from that synthesis slot. Details of the CS8905 micro-instructions and associated parameter data formats are not covered in this document.

The Control Register is a 4-bit write-only register which is comprised of the following control bits:

SSR	0 -	Set Sampling Rate = Crystal Oscillator Frequency/1024.
	1 -	Set Sampling Rate = Crystal Oscillator Frequency/2048 (SSR = 1 selects the slow mode).
IDL	0 -	Normal Operation.
	1 -	All slots are forced to idle mode, independent of the P-RAM contents.
SEL	0 -	Select Access to P-RAM.
	1 -	Select Access to A-RAM.
WR	0 -	Request a Read from P-RAM or A-RAM.
	1 -	Request a Write to P-RAM or A-RAM.

The Control Register is accessed by first performing a Write operation to the CS8905 with address line A2=1 (Address lines A1 and A0 are "don't care" conditions). Note that a change of the Control Register IDL bit from 0 to 1 may take up to 1.5 µs [3 µs in slow mode] to take effect.

To write to the CS8905 P-RAM or A-RAM, the following steps must be taken:

1. Write the desired address to the CS8905
2. Write the data to the CS8905
3. Write to the CS8905 Control Register, setting WR=1
4. Allow 1.5 µs [3 µs in slow mode] for the write cycle to be completed.

To read from the CS8905 P-RAM or A-RAM, the following steps must be taken:

1. Write the desired address to the CS8905
2. Write to the CS8905 Control Register, setting WR=0
3. Allow 1.5 µs [3 µs in slow mode] for the read cycle to be completed.
4. Read the data from the CS8905

The desired address is written to the CS8905 by performing a write cycle with A2A1A0=000. The address formats for P-RAM, A-RAM (SSR bit=0), and A-RAM (SSR bit=1) are each different. These formats are given in Table 1.

The data formats for reading or writing from/to the 19 bit P-RAM and the 15-bit A-RAM are given in Table 2.

The Interrupt Register is an 8-bit read-only register which indicates the slot number and the parameter address which caused the interrupt. The parameter address identifies one parameter location within the 16-parameter P-RAM block associated with a slot. The Interrupt Register is accessed by reading from the CS8905 at address A2A1A0 = 000. Reading the Interrupt Register will not reset the interrupt cause. After initially reading the Interrupt register, the microprocessor should change the slot parameters to remove the interrupt cause, then perform a dummy read of the Interrupt Register (read the register and discard the result) to clear any possible interrupts which may be pending from the same cause. Most musical synthesis applications do not need to utilize the interrupt features of the CS8905.

Type of Address (Read/Written)	Address			Address Data Format							
	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
P-RAM Address	0	0	0	V3	V2	V1	V0	MAD3	MAD2	MAD1	MAD0
A-RAM with SSR=0	0	0	0	AL2	AL1	AL0	PC4	PC3	PC2	PC1	PC0
A-RAM with SSR=1	0	0	0	AL2	AL1	PC5	PC4	PC3	PC2	PC1	PC0

Notes:
1. V0-V3 = Synthesis Slot Number
2. MAD0-MAD3 = Address of specific parameter within the 16 word block associated with the specified slot
3. AL0-AL2 = Algorithm number
4. PC0-PC5 = Address of specified micro instruction within the 32 word block [64 word block in slow mode] associated with the specified algorithm number.

Table 1. Data Format for writing Address Information to the CS8905

Type of Data (Read/Written)	Address			Data Format							
	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
P-RAM data	0	0	1	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	0	B15	B14	B13	B12	B11	B10	B9	B8
	0	1	1	X	X	X	X	X	B18	B17	B16
A-RAM data	0	0	1	I7	I6	I5	I4	I3	I2	I1	I0
	0	1	0	X	I14	I13	I12	I11	I10	I9	I8

Notes:
1. B0-B18 = P-RAM parameter data (19 bit word)
2. I0-I14 = A-RAM micro instruction data (15 bit word)

Table 2. Data Format for reading/writing P-RAM or A-RAM data to CS8905

Sample Memory Interface

The CS8905 provides a 20 bit address bus and 12 bit wide data bus for access to external memory. The memory interface signals are output under micro-instruction control. Therefore, the timing requirements for external memory access are algorithm dependent.

The 20 bit address bus is made up of 8 bits of waveform address information from the WF register, and 12 bits of phase information from the PHI register. The upper 8 bits of the address bus, WA12-WA19, represent the 8 least significant bits of the 9 bit WF register. The lower 12 bits of the address bus, WA0-WA11, represent the 12 most significant bits of the 19 bit PHI register.

The 19 bit PHI register can be subdivided into an integer part and a fractional part. The relative sizes of the integer and fractional parts of the phase will depend on the memory size and memory addressing techniques used in an application. The integer part of the phase is that part of the PHI register which is used to address external memory (12 bits maximum). The fractional part of the phase is that part of the PHI information which does not address external memory (7 bits minimum). The size of the fractional part of the phase affects the playback frequency accuracy in wave table synthesis applications.

The CS8905 is capable of directly addressing a maximum of 1 Msample of external memory. In this case the fractional part of the phase is 7 bits. This provides sufficient frequency resolution for samples which will be replayed without pitch transposition. However, for implementations which will shift the pitch of stored samples during playback, a minimum of 9 bits of fractional phase information is recommended. This limits the memory size for direct addressing to 256 Ksamples. For larger transposable sample memories, a paged address system should be implemented. Transposable sample memory sizes of up to 64 Msamples can be implemented with excellent frequency accuracy using paging. Paging requires only one additional micro-instruction per memory access compared to direct addressing.

Figure 3 depicts a 32K x 8 RAM sampling memory which is directly addressed by the CS8905. In this case, the five lower address lines WA0-WA4 are not used to address sample memory, and the fractional part of the phase is increased to 12 bits.

Figure 4 shows a 1M x 12 bit sample memory which is organized as 4 pages of 256 Ksamples per page. Each page is divided into 512 waves of 512 samples/wave. The address lines WA12 and WA13 are used to select one of the four pages. In this case the wave number (WF register data) is output and captured from address lines WA2-WA10 by the 74HC174 latches on the falling edge of $\overline{WCS}$. The sample address within the page (the integer part of the phase) is then taken from address lines WA3-WA11. The fractional part of the phase has 10 bit resolution, allowing good frequency accuracy. Note that in this example, 12 bit samples are stored in two 8-bit wide ROMs. The smaller 4Mbit ROM holds the 4 lower data bits for two consecutive samples in each of its' 8-bit memory locations. The correct nibble is selected using the 74HC157 based on the state of address line WA3. Address lines WA14-WA19 could be utilized as additional page address bits to expand this addressing mechanism to a maximum of 256 pages (64 Msamples) while maintaining 10 bits of resolution in the fractional part of the phase.

When 8-bit sample memories are utilized, the unused data bus pins on the CS8905 should be pulled down to ground through 10 kOhm resistors.

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For high quality sampling algorithms which employ paged addressing, an external buffer circuit may be added to the memory interface circuitry to allow the CS8905 to perform linear interpolation between sample values read from memory. The buffer is used to selectively gate the lower lines of the CS8905 address bus onto the data bus. This allows the synthesis algorithm to read the most significant bits of the fractional phase information via the data bus for use as a weighting constant in the interpolation calculations.

DAC Interface

The CS8905 DAC interface consists of a left/right clock signal WSBD, a bit clock CLBD and the stereo output data stream DABD. The digital audio output format for the CS8905 is shown in Figure 5. Note that the most significant bit (msb) of the sample is output from the CS8905 1/2 bit time (1/2 clock cycle of the CLBD bit clock) after the rising or falling edge of WSBD. This timing format may be converted to a more common format, wherein the msb is output one full bit time after the edge of CLBD, using either of the two circuits shown in Figure 6.

The digital audio output from the CS8905 has a positive DC offset of 5% of the full scale value. Some low cost DACs generate a considerable amount of electrical noise when transitioning

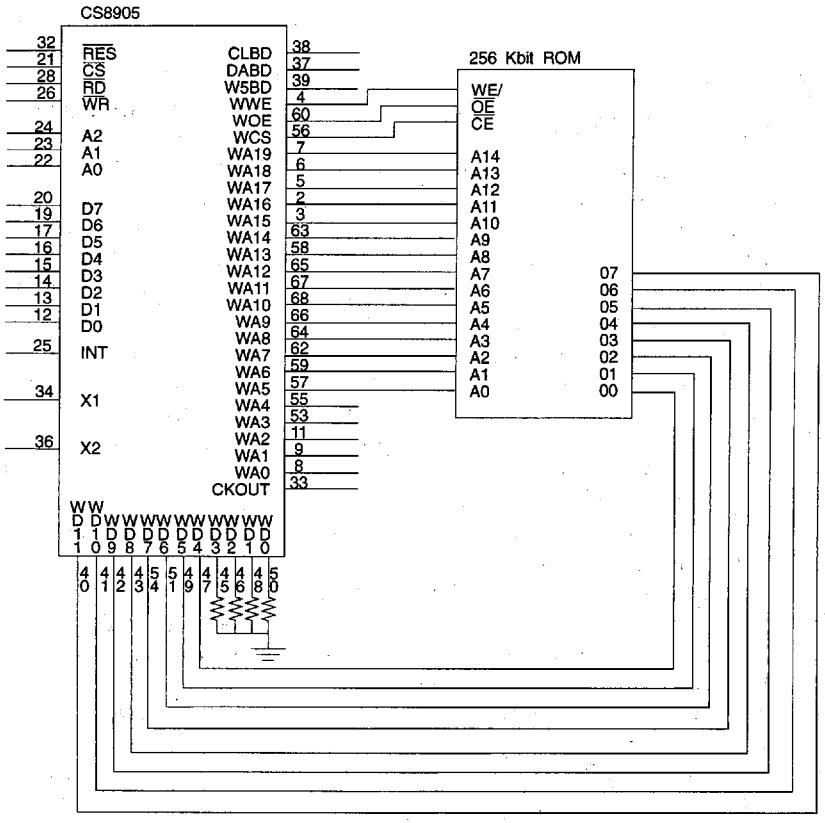


Figure 3. Direct Addressing of 32Kx8 Sample Memory

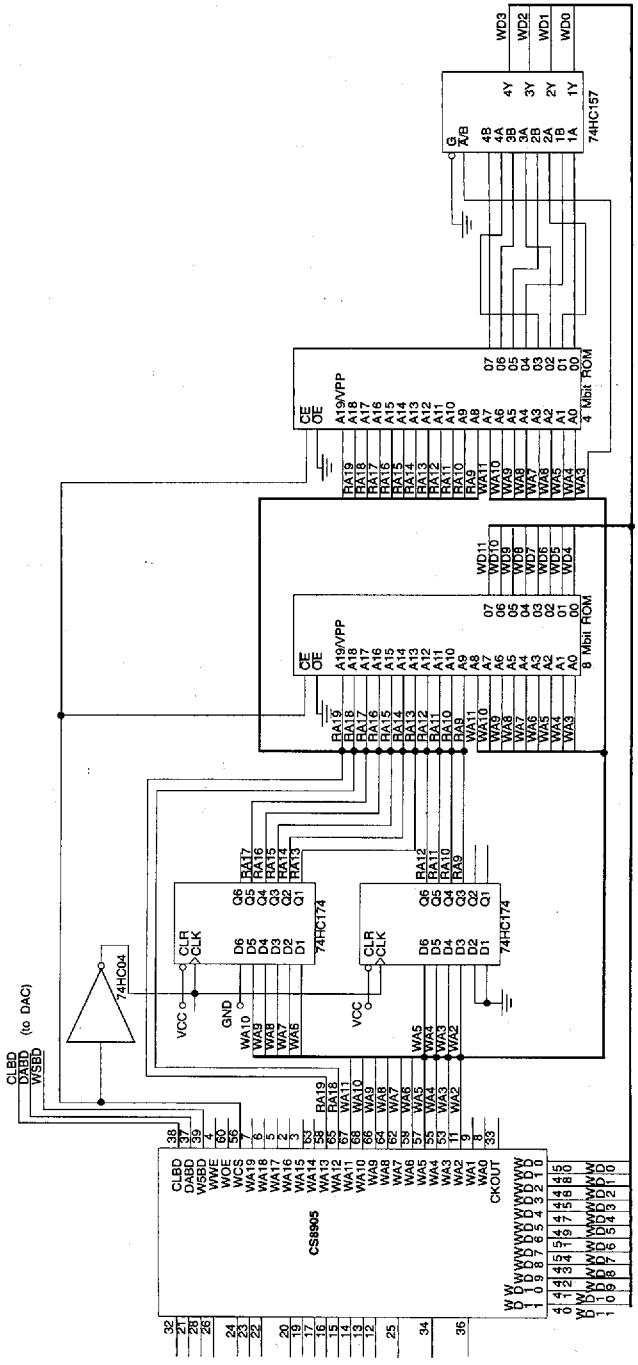


Figure 4. 1Mx12 Sample Memory Using Paging

from zero (an input code of all zeros) to minus one (an input code of all ones). The 5% DC offset can dramatically reduce the signal to noise level for small signals when using this type of DAC. If the digital output from the CS8905 is input to another digital processing device, the offset may be removed by subtracting the value 0D00 Hexadecimal from each sample received from the CS8905.

The ground reference for the DAC should be connected directly to the CS8905 GND at pin 35, and this should be the only connection between analog ground and digital ground.

Oscillator Circuit

The CS8905 timing may be generated using the internal oscillator (external crystal circuit) or using an external oscillator. Trace lengths should be kept to a minimum, and the board layout should include ground plane beneath the oscillator circuit components.

If an external oscillator circuit is utilized, shield the input trace from the oscillator to the CS8905 X1 input and keep the trace lengths to a minimum. The external clock supplied to the X1 pin should be CMOS level. Pin X2 should be left open.

Power Connections and Decoupling

All power and ground pins on the CS8905 device should be connected to the appropriate low impedance supply planes using the shortest trace lengths possible.

Recommended decoupling consists of four 0.1 uF ceramic decoupling capacitors between V_{CC} and GND, one at each of the four sides of the IC. These capacitors should be placed as close to the IC as possible. In addition, place one 10 uF Tantalum capacitor from V_{CC} to GND near the crystal oscillator circuit.

Power-up Reset

The $\overline{\text{RESET}}$ signal initializes the CS8905. The initialization includes the following:

1. Initialize internal master clock phasing
2. Select high sampling rate (sets SSR=0 in the Control Register)
3. Set the general idle bit IDL=1 in the Control Register
4. Force the micro-instruction counter to 31
5. Force the slot number to 0

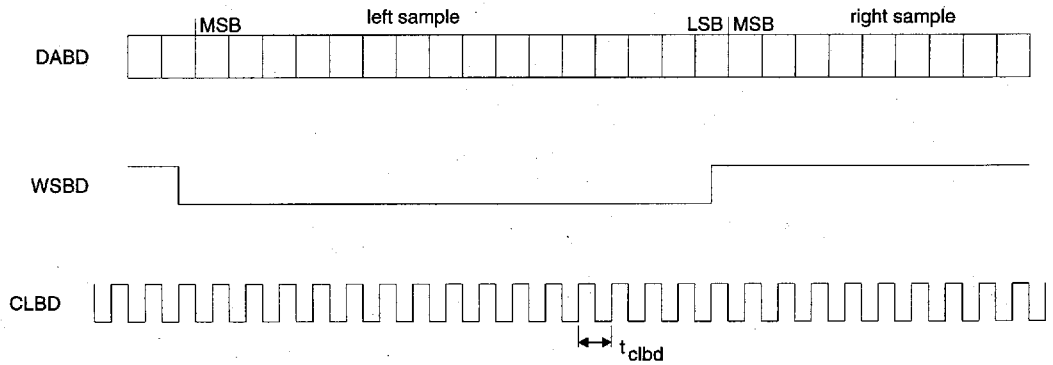


Figure 5. CS8905 Digital Audio Output Format

The $\overline{\text{RESET}}$ input must be held low until the oscillator circuit has stabilized. The CS8905 internal oscillator is enabled during $\overline{\text{RESET}}$, other functions of the device are held in an idle mode while $\overline{\text{RESET}}$ is low.

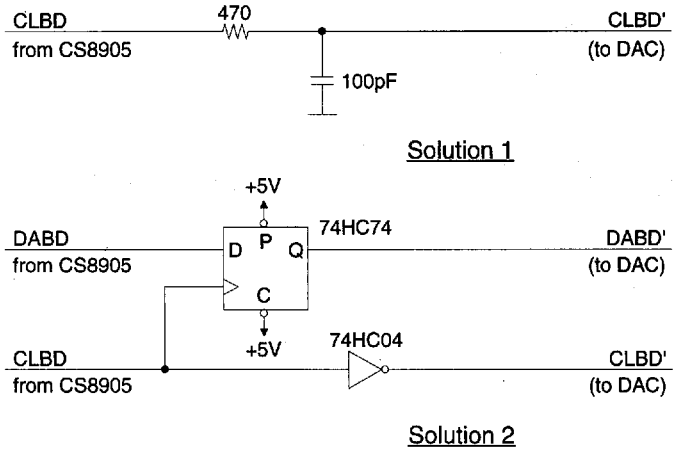
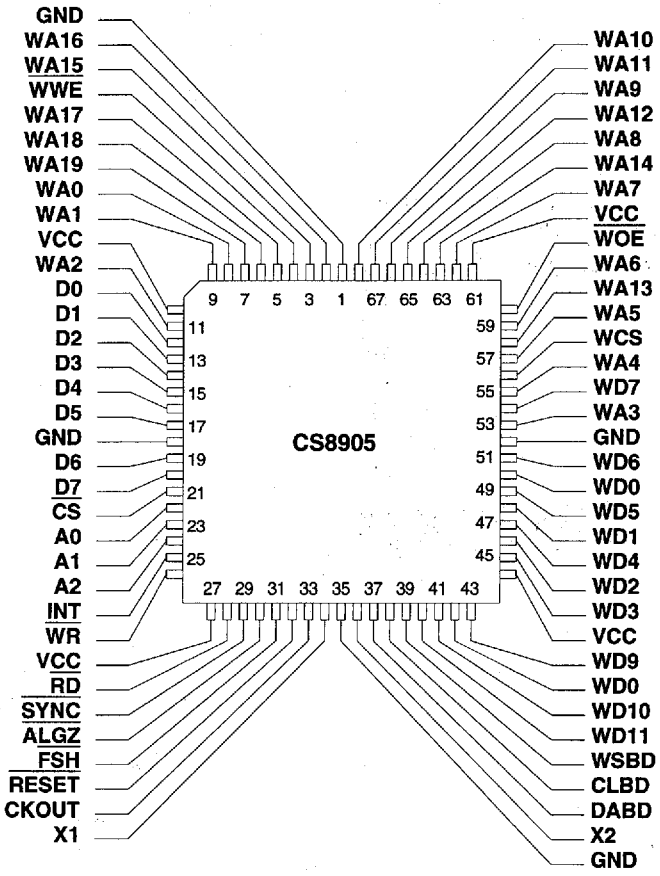


Figure 6. Digital Audio Output Format Conversion

PIN DESCRIPTIONS



Pins

GND - Ground. PINS 1, 18, 35, and 52.
Ground, all ground pins on the device must be connected to a low impedance ground.

VCC - +5V supply. PINS 10, 27, 44, and 61.
+5V supply, all VCC pins on the device must be connected to a low impedance +5V supply.

D0-D7 - Data I/O. PINS 12, 13, 14, 15, 16, 17, 19, and 20.
These bi-directional data lines are used to transfer data between an external microprocessor and the CS8905.

A0-A2 - Address Select Input from Microprocessor. PINS 22, 23, and 24.
These pins allow an external microprocessor to select the CS8905 control register or specify data registers for read/write operations.

$\overline{CS}$ - Chip Select Input. PIN 21.
This is the CS8905 chip select input from an external microprocessor. Active low.

$\overline{RD}$ - Read Strobe Input from Microprocessor. PIN 28.
This signal is the read strobe from an external microprocessor. Active low.

$\overline{WR}$ - Write Strobe Input from Microprocessor. PIN 26.
This signal is the write strobe from an external microprocessor. Active low.

$\overline{INT}$ - Interrupt Request Output to Microprocessor. PIN 25.
This output will be driven low by the CS8905 to interrupt an external microprocessor.

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X1 - Xtal or External Clock Input. PIN 34.
This is the input pin for the internal oscillator circuit. A crystal or external clock frequency of 48 MHz maximum may be connected. If an external oscillator is used, it should be CMOS logic level.

X2 - Xtal Output Connection. PIN 36.
This pin is the internal oscillator circuit output. If an external oscillator is used, this pin should be left open.

CKOUT - Output Clock. PIN 33.
This output clock has a frequency equal to the CS8905 oscillator frequency divided by four.

$\overline{RESET}$ - Chip Reset Input. PIN 32.
This active low input is used to reset and initialize the CS8905. This signal should be held low for at least 10 ms after power up.

DABD - Serial Data Out to External DAC. PIN 37.
This signal is the stereo 16-bit digital audio data output from the CS8905 to an external DAC.

CLBD - Clock Output to External DAC. PIN 38.
This output is the bit clock for the DABD signal.

WSBD - Left/Right Channel Select Output to External DAC. PIN 39.
This is the left/right word clock for the DABD signal.

WA0-WA19 - External Sampling Wave Memory Address Output. PINS 8, 9, 11, 53, 55, 57, 59, 62, 64, 66, 68, 67, 65, 58, 63, 3, 2, 5, 6, and 7
These address lines are used to address an external sample memory.

WD0-WD11 - External Sampling Wave Memory Data Output. PINS 50, 48, 46, 45, 47, 49, 51, 54, 43, 42, 41, and 40.

These data lines are used to pass sample data from/to external sample memory.

$\overline{WCS}$ - External Sampling Wave Memory Chip Select Output. PIN 56.

This is an active low chip select signal for external sample memory.

$\overline{WOE}$ - External Sampling Wave Memory Output Enable. PIN 60.

This signal is an active low output enable strobe pin for external sample memory.

$\overline{WWE}$ - External Sampling Wave Memory Write Output. PIN 4.

This signal is an active low write strobe for external RAM sample memory.

$\overline{SYNC}$ - Synchronize Input. PIN 29.

This active low signal is used for synchronization between several CS8905 devices. This signal should be tied to V_{CC} under normal operating conditions.

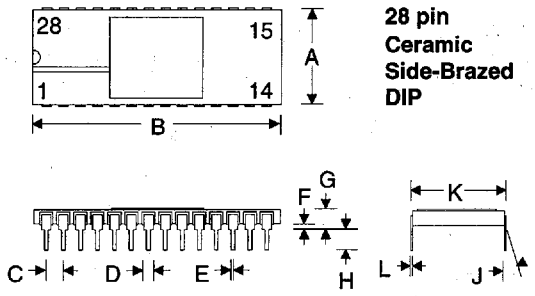
$\overline{ALGZ}$ - Zero Algorithm Input. PIN 30.

This active low signal will force execution of algorithm zero. This signal should be tied to V_{CC} under normal operating conditions.

$\overline{FSH}$ - Fast Shift Input. PIN 31.

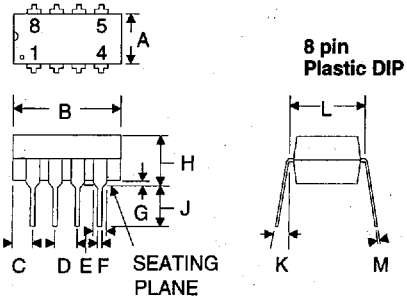
This active low input signal forces the serial data DABD to be shifted out at the master clock rate rather than the CLBD rate. This signal should be tied to V_{CC} under normal operating conditions.

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

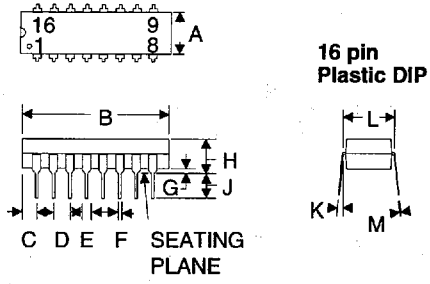
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



8 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

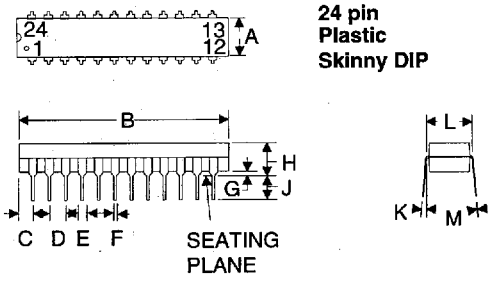
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

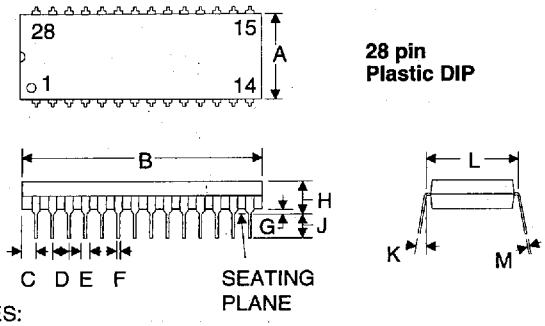
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

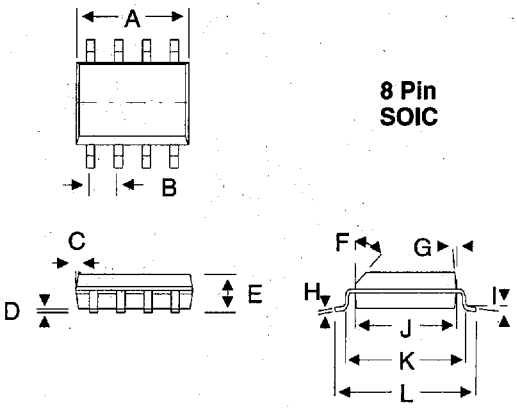
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

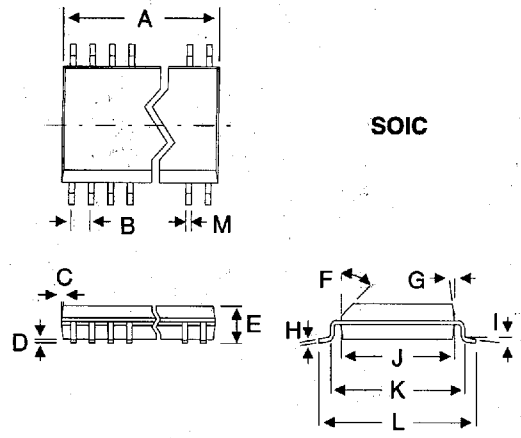
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



8 Pin SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

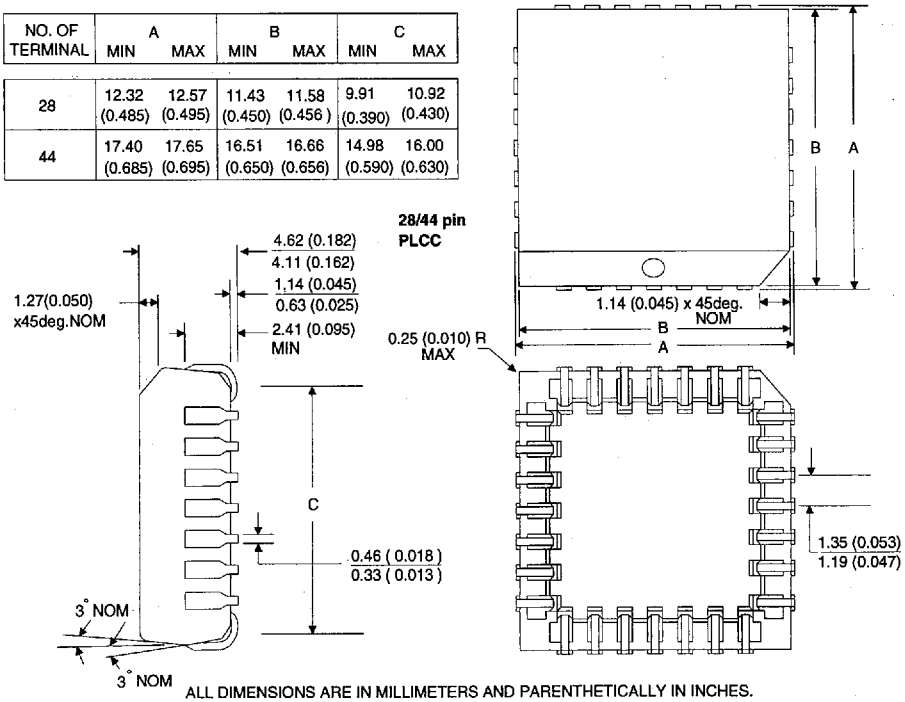


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

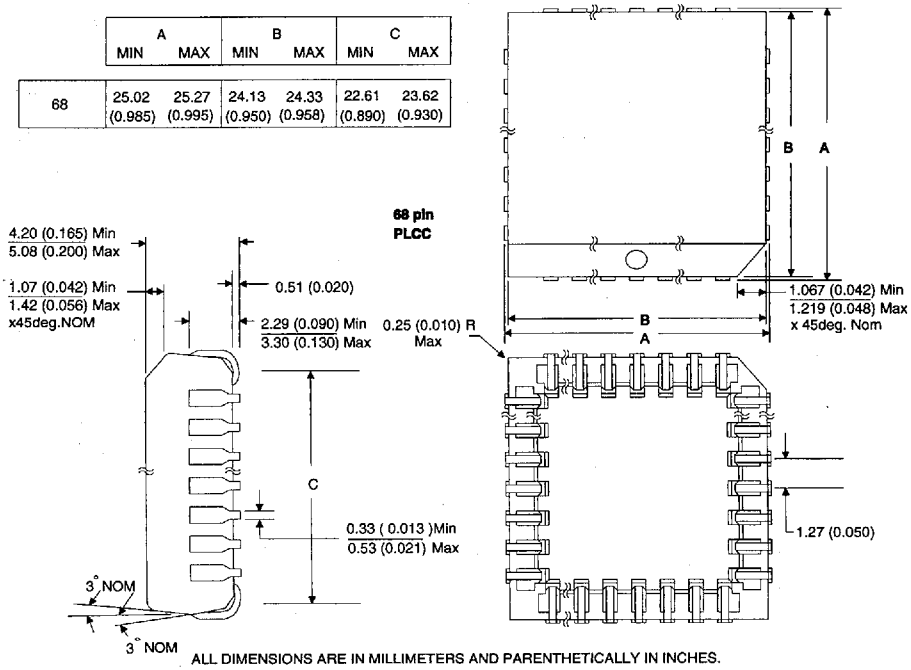
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

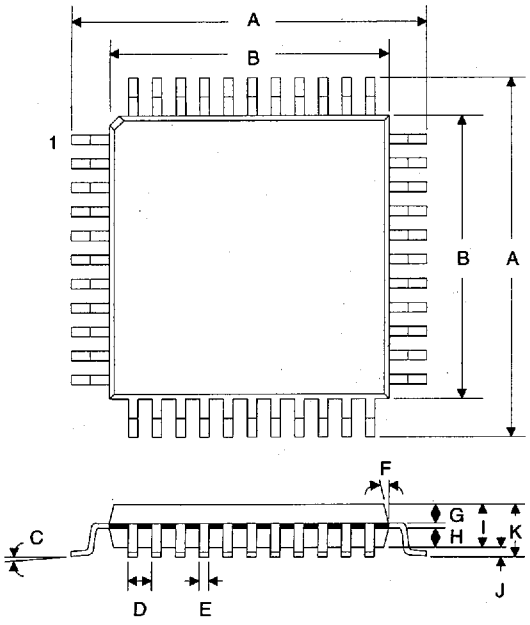
	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

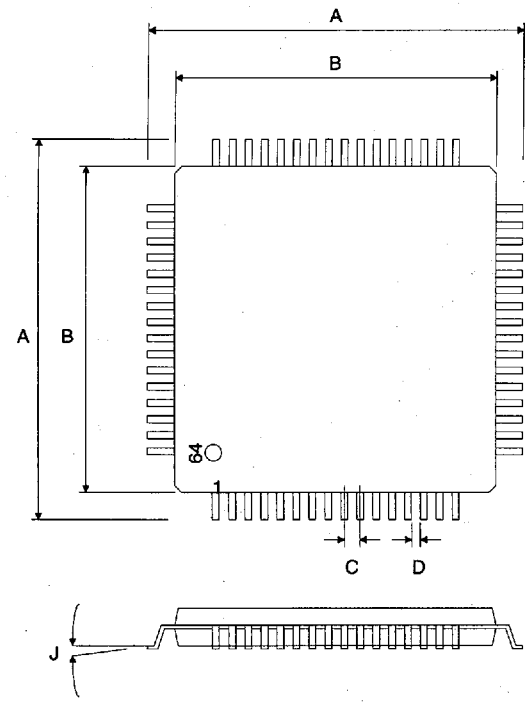
11

44 PIN QUAD FLATPACK



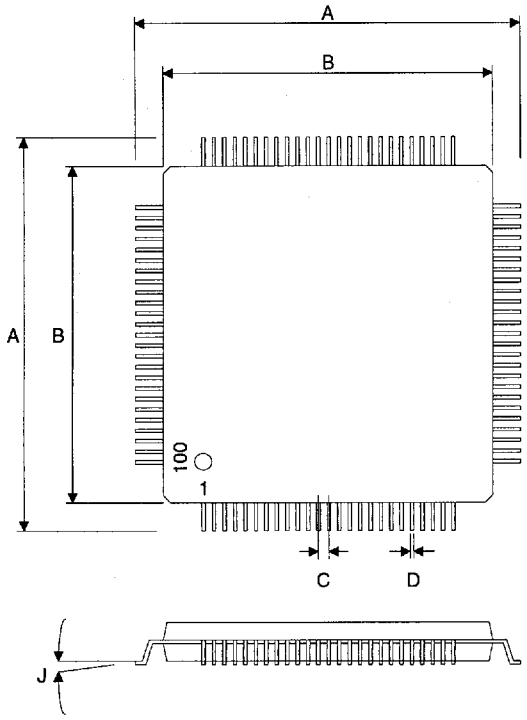
0.102 MAX
Lead Coplanarity

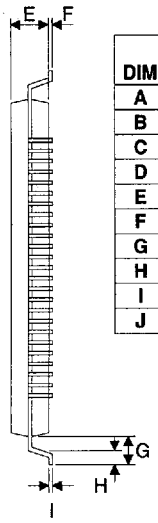
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026



64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

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