DRAM

256K x 4 DRAM

FAST PAGE MODE

AVAILABLE AS MILITARY SPECIFICATION

- SMD 5962-90617
- MIL-STD-883

FEATURES

- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- Optional FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- 512-cycle refresh distributed across 8ms
- Specifications guaranteed over full military temperature range (-55°C to +125°C)

OPTIONS MARKING

- Timing

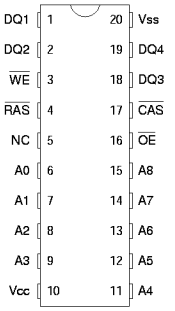
80ns access	- 8
100ns access	-10
120ns access	-12

- Packages

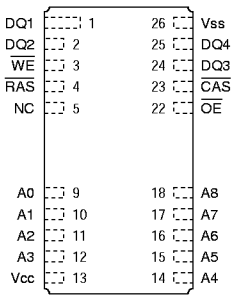
Ceramic DIP (300 mil)	C	No. 103
Ceramic LCC	EC	No. 202

PIN ASSIGNMENT (Top View)

20-Pin DIP (D-8)



20-Pin LCC



GENERAL DESCRIPTION

The MT4C4256 883C is a randomly accessed solid-state memory containing 1,048,576 bits organized in a 262,144 x4 configuration. During READ or WRITE cycles, each 4-bit word is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode.

During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins (Qs) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the outputs (Qs), the outputs are activated and retain the selected cells' data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four leads using common I/O, and information direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

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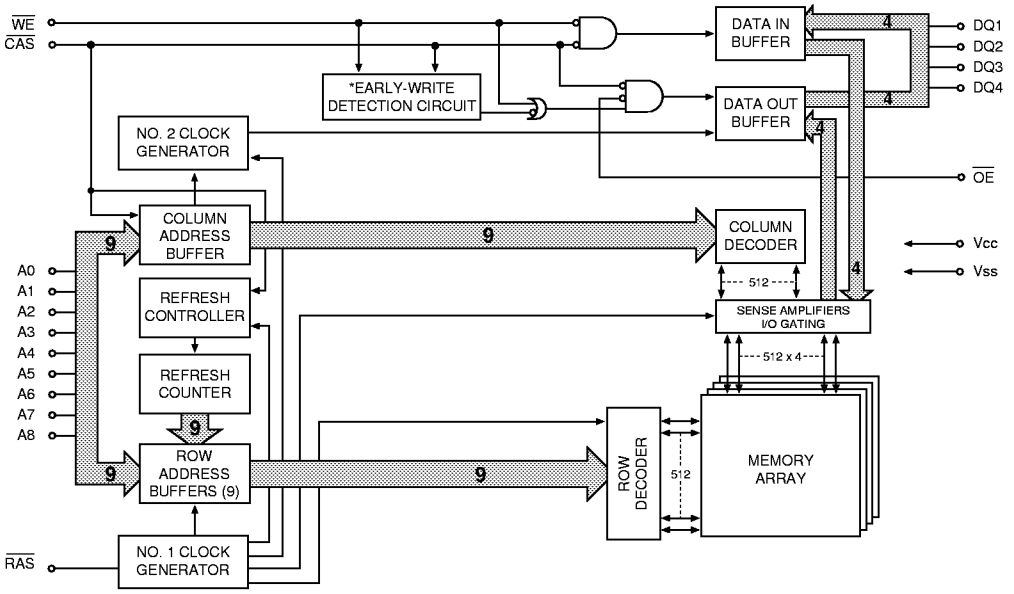
FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1.5V to +7.0V
Storage Temperature Range ..... -65°C to +150°C
Power Dissipation 1W
Lead Temperature (Soldering 5 Seconds) ..... 270°C
Junction Temperature (T_J) ..... +175°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes: 1, 6, 7) (-55°C ≤ T_C ≤ +125°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+.5	V	
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-.5	0.8	V	
INPUT LEAKAGE CURRENT Any Input (0V ≤ V_{IN} ≤ 6.5V), All other pins not under test = 0V	I_I	-5	5	µA	
OUTPUT LEAKAGE CURRENT (Q is Disabled, 0V ≤ V_{OUT} ≤ 6.5V)	I_{OZ}	-5	5	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	3	3	3	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V; all other inputs = V_{CC}-0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	70	60	50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	50	40	30	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	70	60	50	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	70	60	50	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: (A0-A8), D	C_{I1}		7	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: (DQ1-DQ4)	C_O		8	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T_C ≤ +125°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	150		180		210		ns	
READ-WRITE cycle time	^tRWC	195		235		275		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		55		65		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		110		130		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Output Enable	^tOE		20		25		30	ns	23
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		50		60	ns	
$\overline{RAS}$ pulse width	^tRAS	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		80		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	25	100,000	30	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		12		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		12		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	20	60	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		80		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T_C ≤ +125°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^tOFF	0	20	0	20	0	25	ns	20, 26
Output disable	^tOD		20		20		25	ns	26
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		70		80		ns	
Write command pulse width	^tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		80		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	105		125		150		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	65		75		90		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	45		50		60		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		20		25		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		25		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	24

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T_C ≤ +125°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns. This parameter is not measured.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data outputs (DQs) are High-Z.
12. If $\overline{CAS}$ = V_{IL}, data outputs (DQs) may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQs will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

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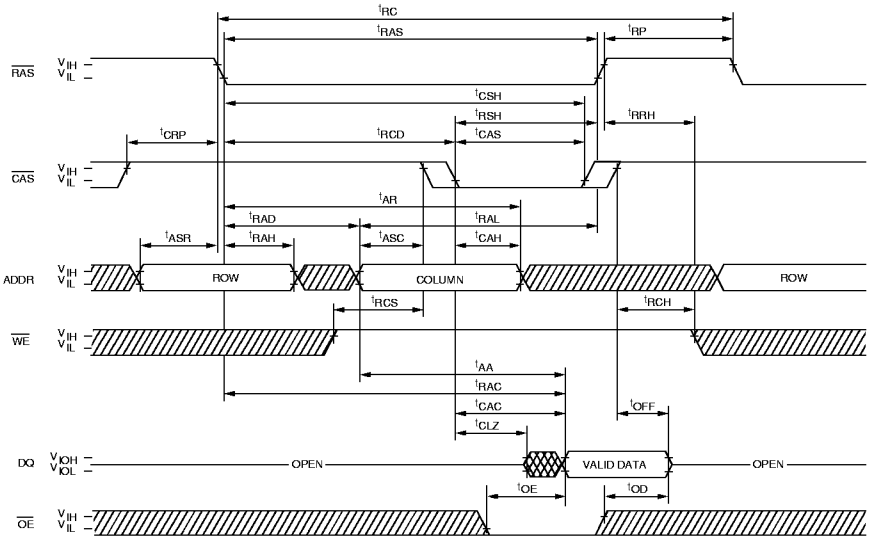
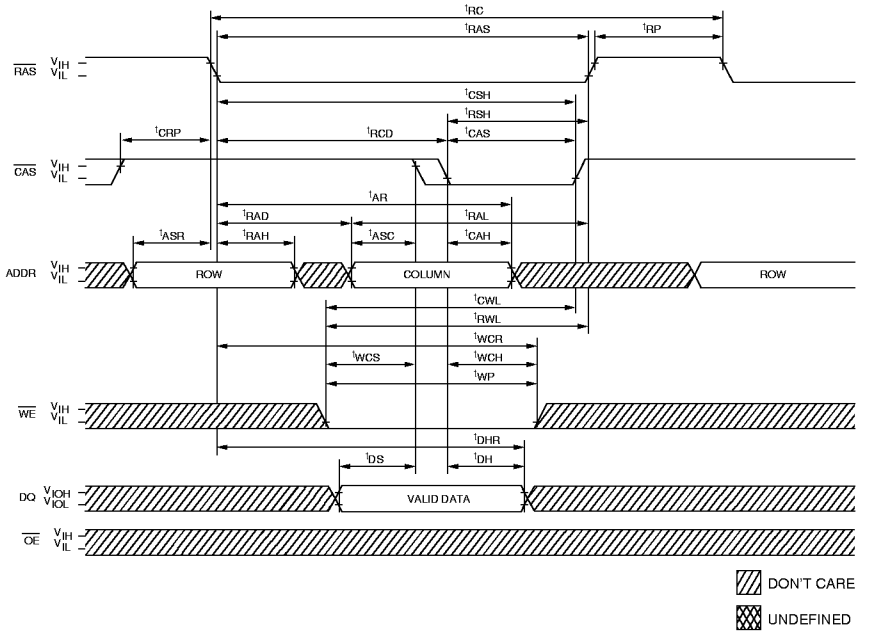
READ CYCLE



EARLY-WRITE CYCLE



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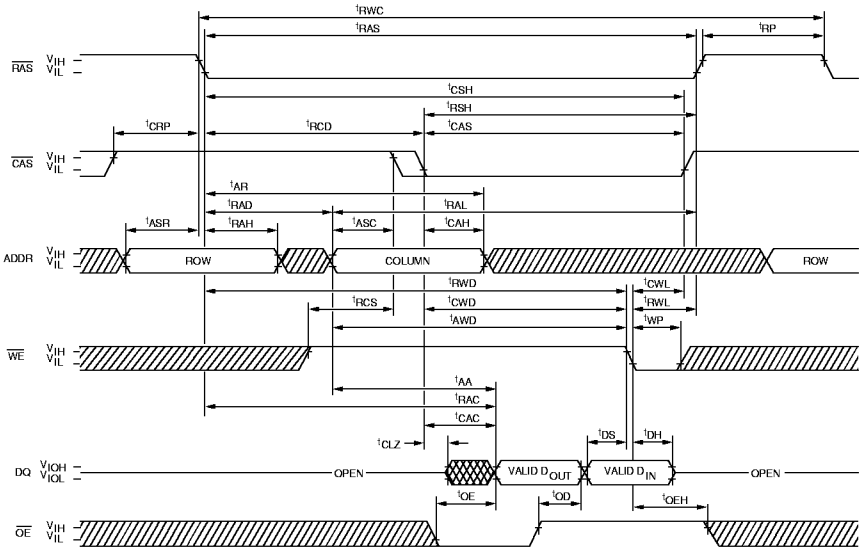
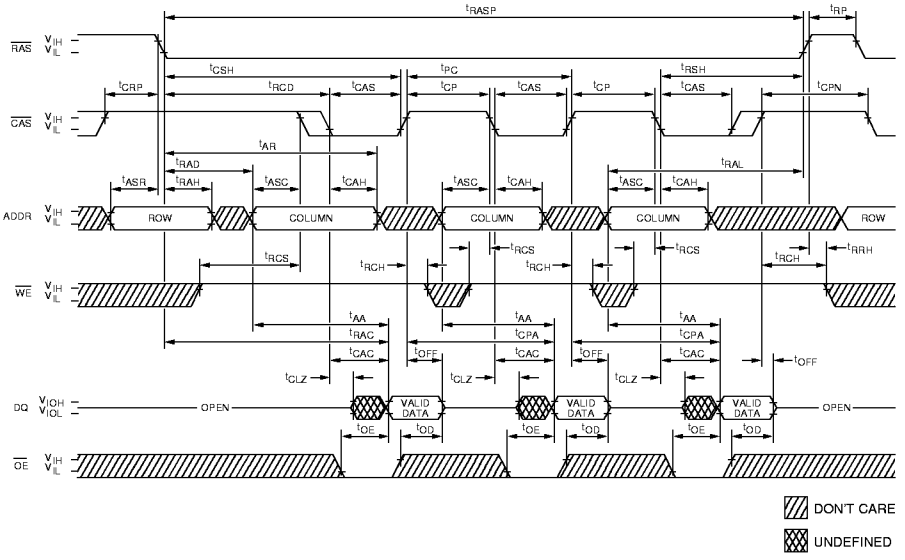
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE



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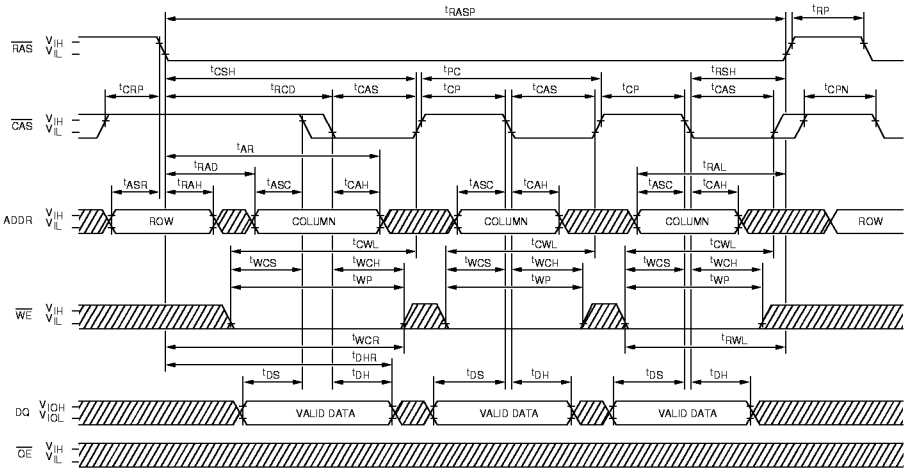
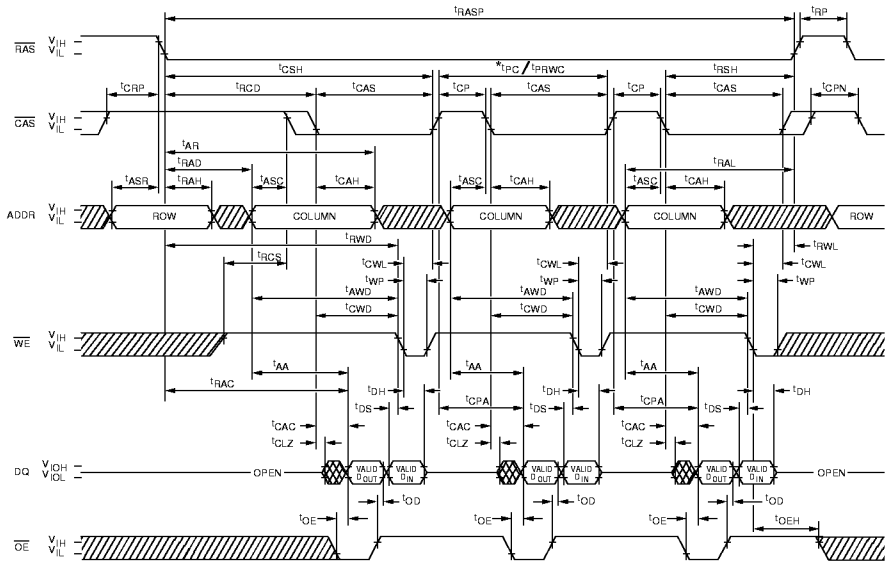
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



* tPC = LATE-WRITE cycle
tPRWC = FAST READ-MODIFY-WRITE cycle

DON'T CARE
UNDEFINED

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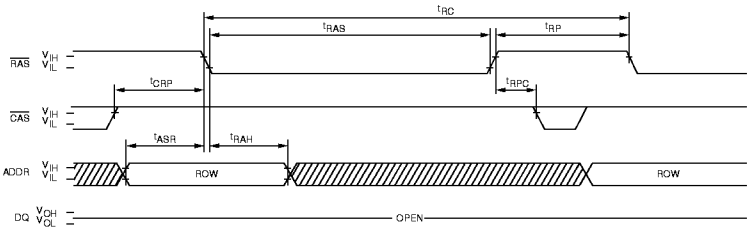
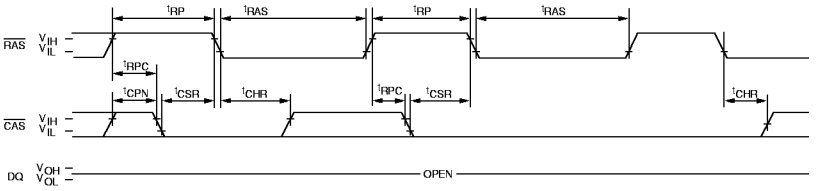
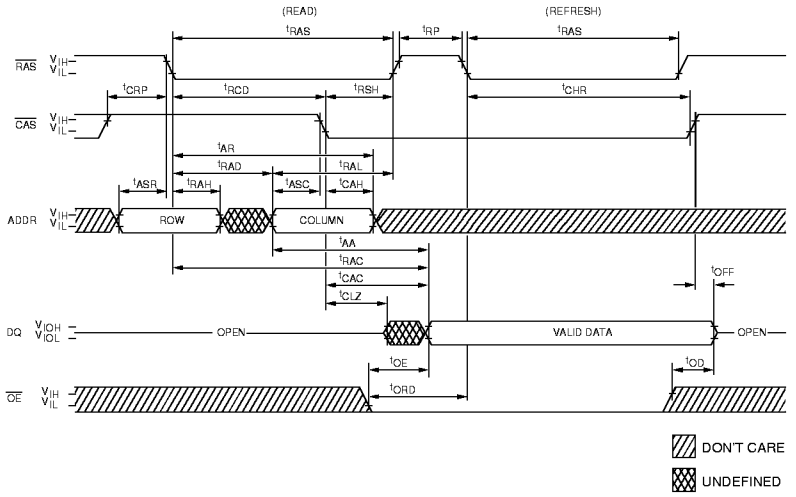
$\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH, $\overline{OE}$ = LOW)



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ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

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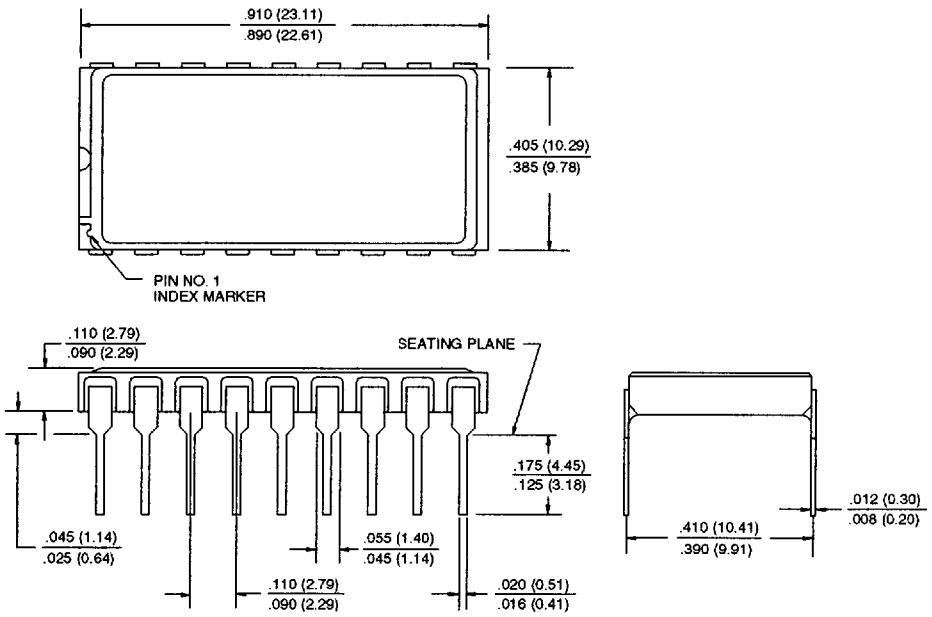
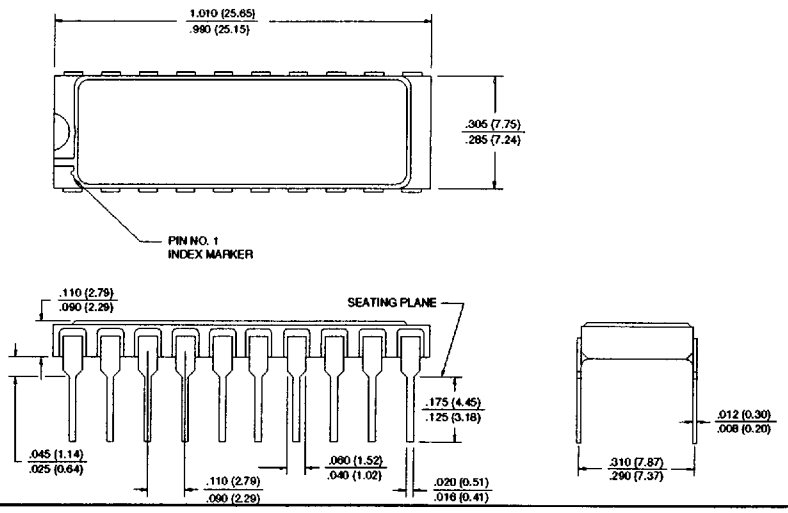
PACKAGE NO. 102
18 CDIP (400 mils)



PACKAGE NO. 103
20 CDIP D-8 (300 mils)



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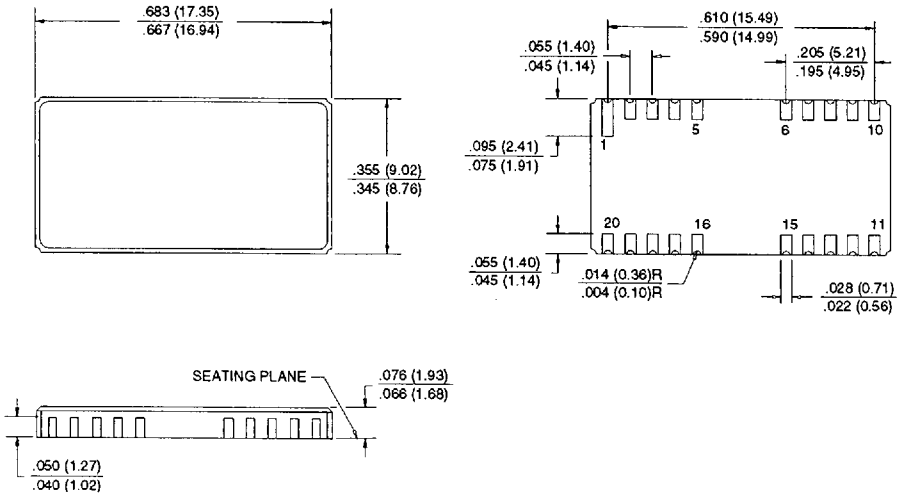
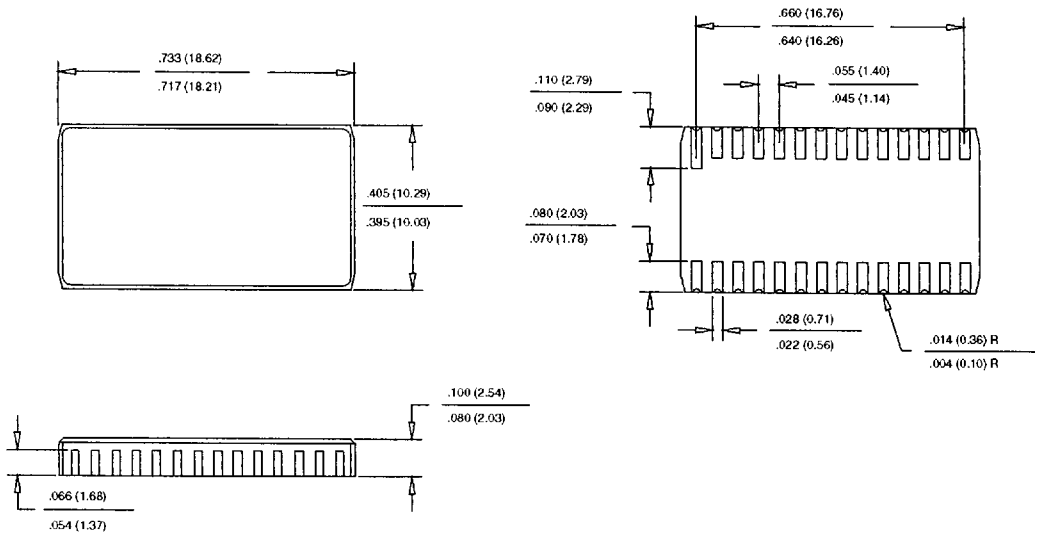
PKG-2

9002117 0000952 875

PACKAGE NO. 202
20 CLCC



PACKAGE NO. 203
28 CLCC



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PKG-9

9002117 0000959 12T