KMM491000/KMM591000

SAMSUNG
Semiconductor

□ 1M × 9 DRAM SIP and SIMM Memory Modules

GENERAL DESCRIPTION

The Samsung KMM491000 and KMM591000 are 1M x 9 dynamic RAM high density memory modules. The ninth bit is generally used for parity and is controlled by $\overline{CAS9}$. Samsung's 1M x 9 memory modules consist of nine KM41C1000 DRAMS in 20-pin SOJ packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The 1M x 9 DRAM modules are available in two package styles. The KMM491000 is a SIP with leads suitable for through hole mounting or for mounting in a socket. The KMM591000 is a SIMM with edge connections and are intended for mounting into 30 pin edge connector sockets.

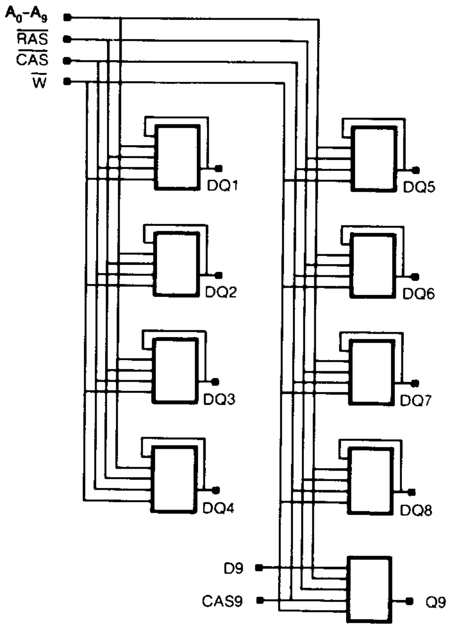
FEATURES

- 1,048,576 × 9-bit Organization
- Ninth device has separate D, Q and $\overline{CAS}$ for Parity applications.
- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}
KMM491000-10	100ns	25ns	190ns
KMM591000-10	100ns	25ns	190ns
KMM491000-12	120ns	30ns	220ns
KMM591000-12	120ns	30ns	220ns

- Page Mode capability
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Single +5V ± 10% power supply
- 512 cycles/8ms refresh

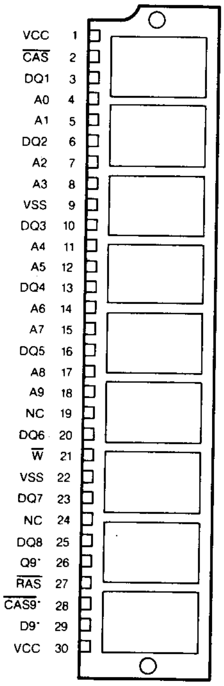
FUNCTIONAL BLOCK DIAGRAM



Part Numbers

KMM491000-10	100ns	SIP	Page Mode
KMM491000-12	120ns	SIP	Page Mode
KMM591000-10	100ns	SIMM	Page Mode
KMM591000-12	120ns	SIMM	Page Mode

PIN CONFIGURATION



*FOR PARITY BIT

Pin Name	Pin Function
A_0-A_9	Address Input
D9	Data In
Q9	Data Out
DQ	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{CAS9}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	5.4	W
Short Circuit Output Current	I_{OS}	50	mA

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Operating Current* (RAS and CAS cycling @ t_{RC} = min.)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC1}	— —	540 450	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	18	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @ t_{RC} = min.)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC3}	— —	540 450	mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling: t_{PC} = min.)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC4}	— —	360 270	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		I_{CC6}	—	9	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min.)	KMM491000-10, KMM591000-10 KMM491000-12, KMM591000-12	I_{CC7}	— —	540 450	mA mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test = 0 volts.)		I_{IL}	-90	90	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH} = 5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5}, and I_{CC7} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE (T_A = 25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0 - A_9, $\overline{W}$, $\overline{CAS}$. $\overline{RAS}$)	C_{IN1}	—	60	pF
Input Capacitance (D_9, $\overline{CAS_9}$)	C_{IN2}	—	7	pF
Input Capacitance (DQ_1 - DQ_8)	C_{DQ}	—	15	pF
Output Capacitance (Q_9)	C_{Q9}	—	10	pF

AC CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%, see notes 1,2)

		KMM491000-10 KMM591000-10		KMM491000-12 KMM591000-12			
	Symbol	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Standard Operation							
Random read or write cycle time	t_{RC}	190		220		ns	
Access time from RAS	t_{RAC}		100		120	ns	3,4
Access time from CAS	t_{CAC}		25		30	ns	4,4
Access time from column address	t_{AA}		50		60	ns	3,10
Access time from CAS precharge	t_{CPA}		55		65	ns	3
CAS to output in Low-Z	t_{CLZ}	5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
RAS precharge time	t_{RP}	80		90		ns	
RAS pulse width	t_{RAS}	100	10,000	120	10,000	ns	
RAS hold time	t_{RSH}	25		30		ns	
CAS precharge time	t_{CPN}	15		20		ns	
CAS hold time	t_{CSH}	100		120		ns	
CAS pulse width	t_{CAS}	25	10,000	30	10,000	ns	
RAS to CAS delay time	t_{RCD}	25	75	25	90	ns	4,5
RAS to column address delay time	t_{RAD}	20	50	20	60	ns	10
CAS to RAS precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to RAS	t_{AR}	95		115		ns	
Column address to RAS lead time	t_{RAL}	50		60		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to CAS	t_{RCH}	0		0		ns	8
Read command hold time referenced to RAS	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	20		25		ns	
Write command hold time referenced to RAS	t_{WCR}	95		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to RAS lead time	t_{RWL}	25		30		ns	
Write command to CAS lead time	t_{CWL}	25		30		ns	
Data-in set-up time	t_{DS}	0		0		ns	9
Data-in hold time	t_{DH}	20		25		ns	9
Data-in hold time referenced to RAS	t_{DHR}	95		115		ns	
Refresh period (512 cycles)	t_{REF}		8		8	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
CAS to write enable delay	t_{CWD}	25		30		ns	7
CAS setup time (CAS-before-RAS refresh)	t_{CSR}	10		10		ns	
CAS hold time (CAS-before-RAS refresh)	t_{CHR}	30		30		ns	

AC CHARACTERISTICS
(Continued)

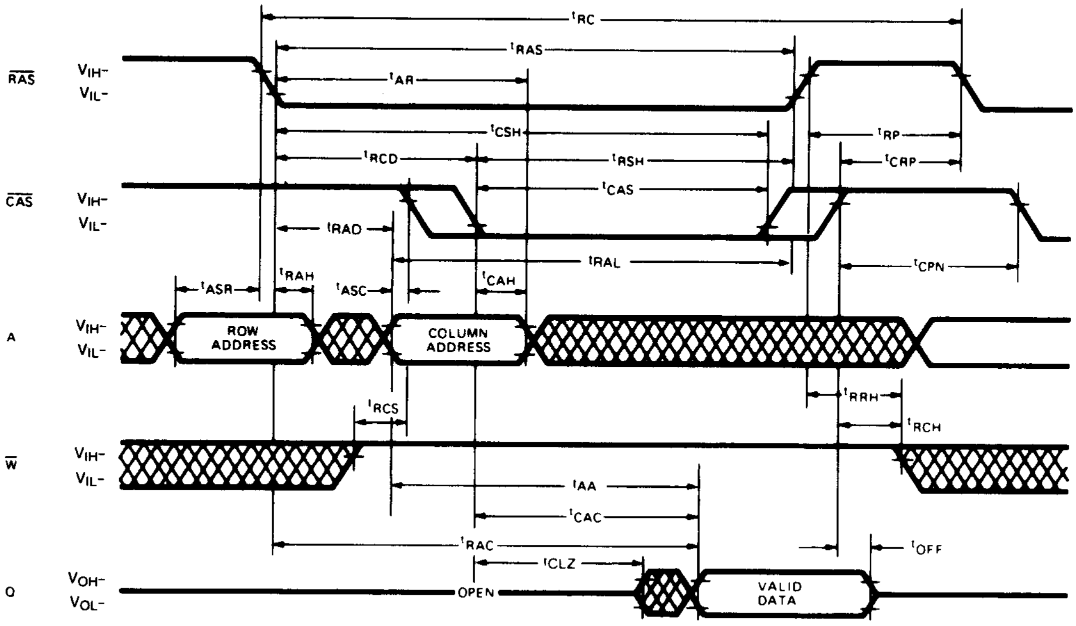
		KMM491000-10 KMM591000-10		KMM491000-12 KMM591000-12			
	Symbol	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	50		60		ns	
Fast page mode cycle time	t_{PC}	60		70		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		15		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	100	100,000	120	100,000	ns	

Notes:

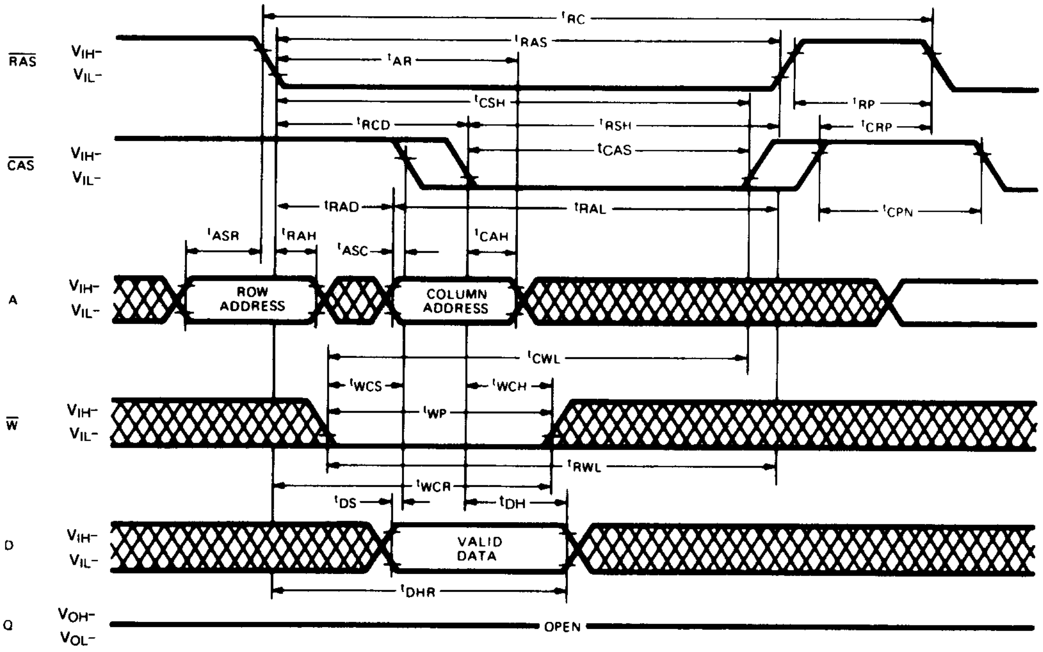
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early write cycle and the data output pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD} (max) limit insures that t_{RCD} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE



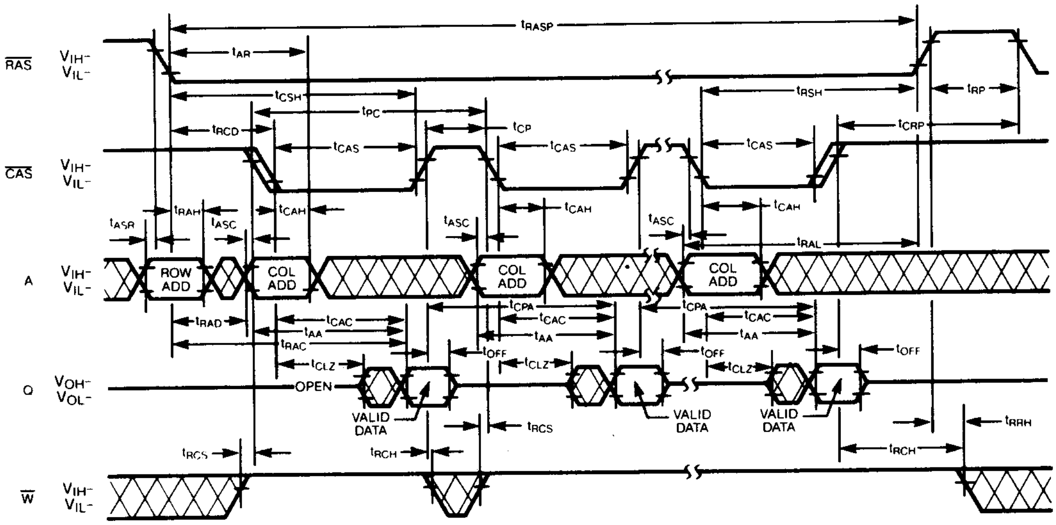
WRITE CYCLE (EARLY WRITE)



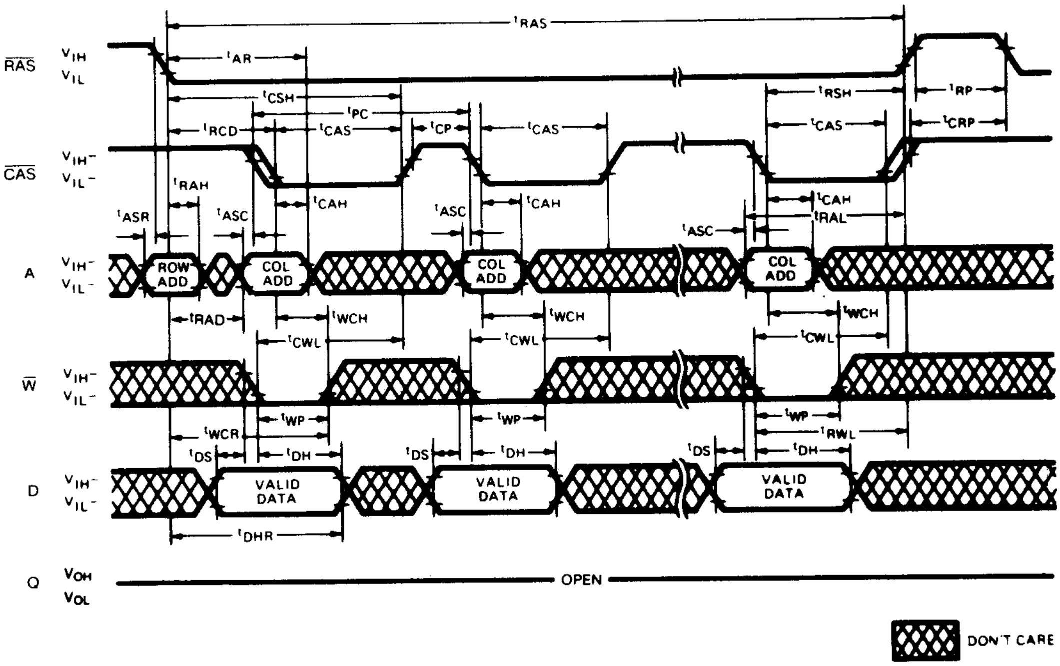
▨ DON'T CARE

TIMING DIAGRAMS
(Continued)

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS
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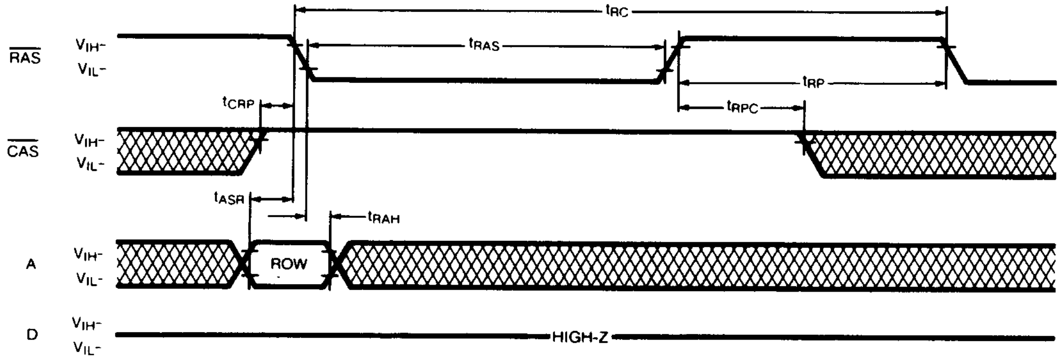
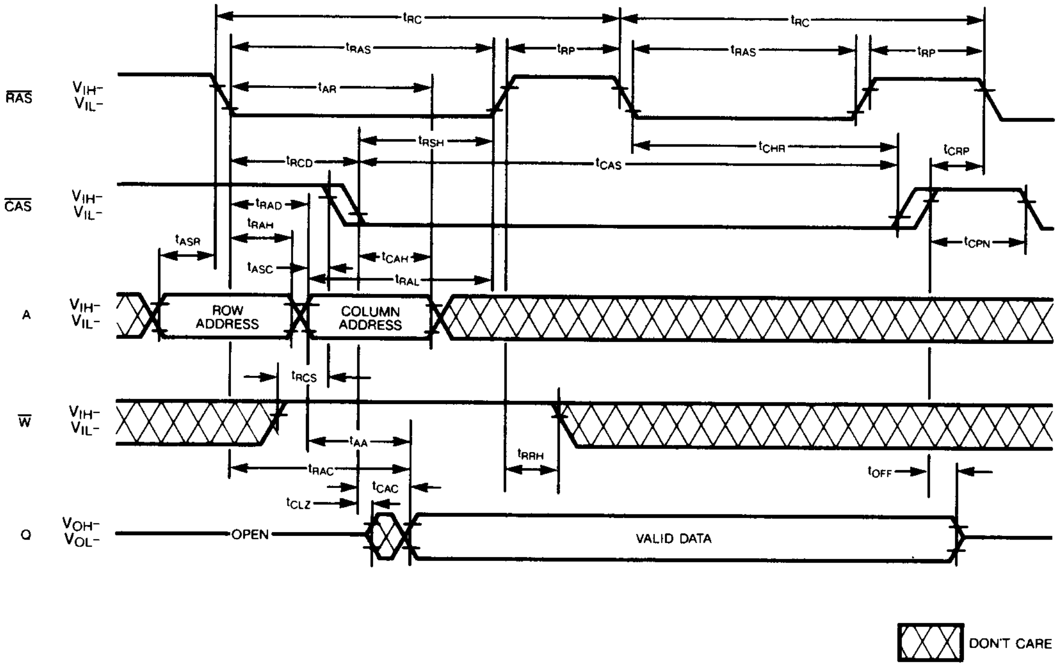
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}; $\overline{W}$, D, A_9 = DON'T CARE



HIDDEN REFRESH CYCLE



TIMING DIAGRAMS
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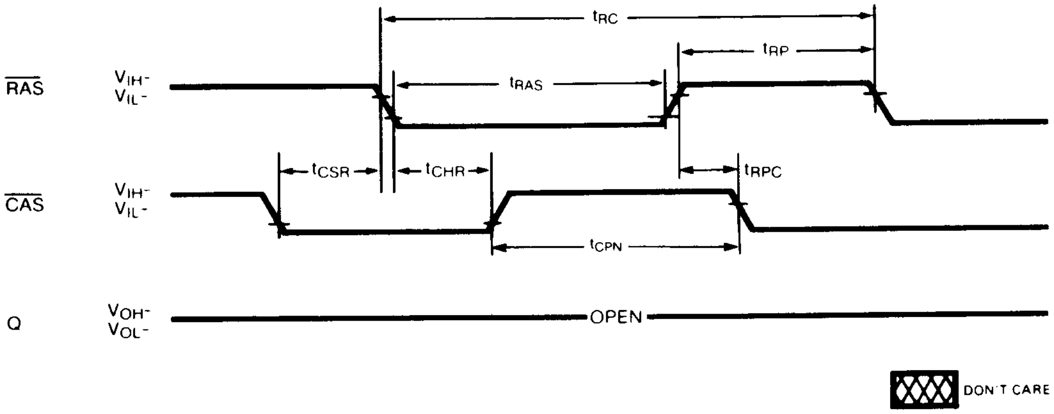
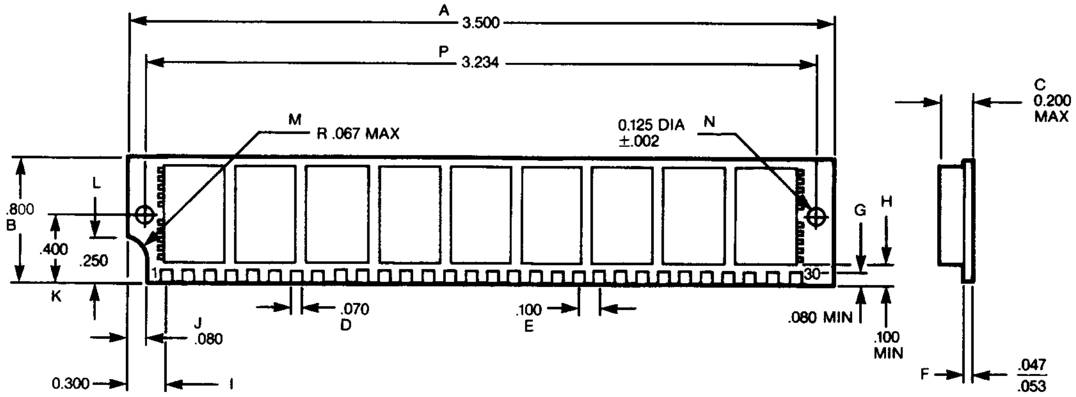
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

NOTE: Address, $\overline{\text{W}}$, D = DON'T CARE



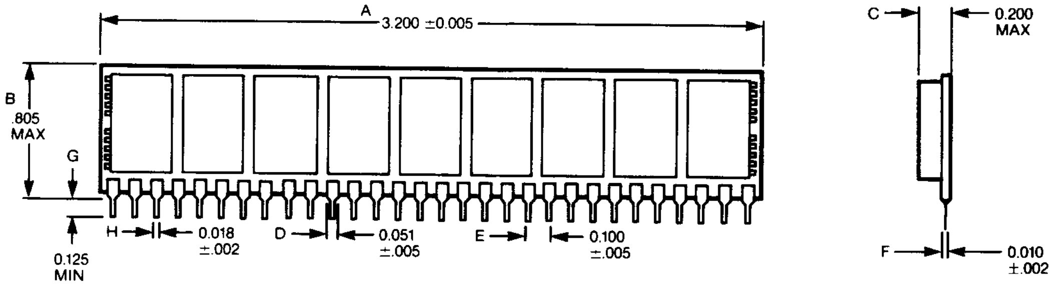
PACKAGE DIMENSIONS

KMM591000 1M × 9 SIMM



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

KMM491000 1M × 9 SIP



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