CS4245

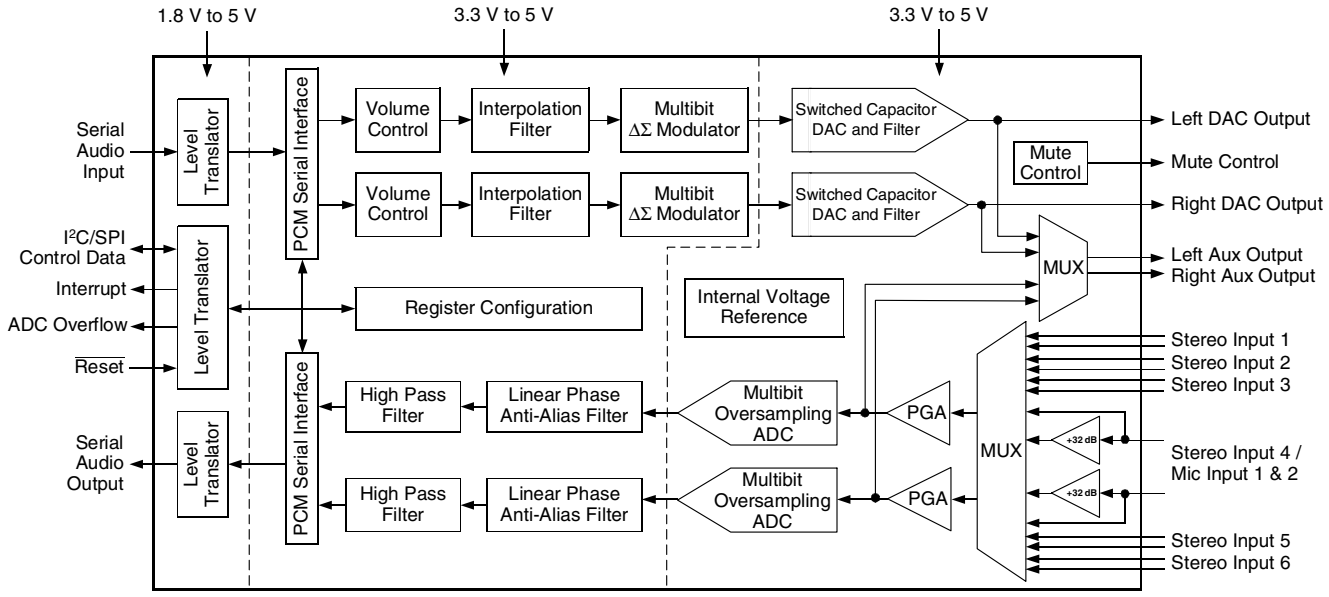
105 dB, 24-Bit, 192 kHz Stereo Audio CODEC

D/A Features

- Multi-bit Delta Sigma modulator
- 105 dB dynamic range
- -95 dB THD+N
- Up to 192 kHz sampling rates
- Single-ended analog architecture
- Volume control with soft ramp
  - 0.5 dB step size
  - Zero crossing click-free transitions
- Popguard™ Technology
  - Minimizes the effects of output transients
- Filtered line level outputs
- Selectable serial audio interface formats
  - Left justified up to 24-bit
  - I²S up to 24-bit
  - Right justified 16, 18, 20 and 24-bit
- Selectable 50/15 µs de-emphasis
- Control Output for External Muting

A/D Features

- Multi-bit Delta Sigma modulator
- 105 dB dynamic range
- -95 dB THD+N
- Stereo 6:1 Input Multiplexer
- Programmable Gain Amplifier (PGA)
  - +/- 12 dB gain, 0.5 dB step size
  - Zero crossing, click-free transitions
- Stereo microphone inputs
  - +32 dB gain stage
  - Low noise bias supply
- Up to 192 kHz sampling rates
- Selectable serial audio interface formats
  - Left justified up to 24-bit
  - I²S up to 24-bit
- High pass filter or DC offset calibration



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

System Features

- Direct interface with 1.8 V to 5 V logic levels
- Optional asynchronous serial port operation
  - Each serial port supports master or slave operation
- Selectable auxiliary analog output
  - Allows analog monitoring of either the ADC input signal after PGA or DAC output signal
- Internal digital loopback
- Power down mode
  - Available for A/D, D/A, CODEC, Mic Preamplifier
- +3.3 V to +5 V analog power supply
- +3.3 V to +5 V digital power supply
- Supports I²C and SPI control port interfaces
- Pin-compatible with CS5345

General Description

The CS4245 is a highly integrated stereo audio CODEC. The CS4245 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

A 6:1 stereo input multiplexer is included for selecting between line level or microphone level inputs. The microphone input path includes a +32 dB gain stage and a low noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain/attenuation of ±12 dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 192 kHz in either slave or master mode.

The D/A converter is based on a 4th-order multi-bit delta sigma modulator with an ultra-linear low pass filter and offers a volume control that operates with a 0.5 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

Standard 50/15 µs de-emphasis is available for a 44.1 kHz sample rate for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4245 and other devices operating over a wide range of logic levels.

ORDERING INFORMATION

CS4245-CQZ	-10° to 70° C	48-pin LQFP
CDB4245		Evaluation Board

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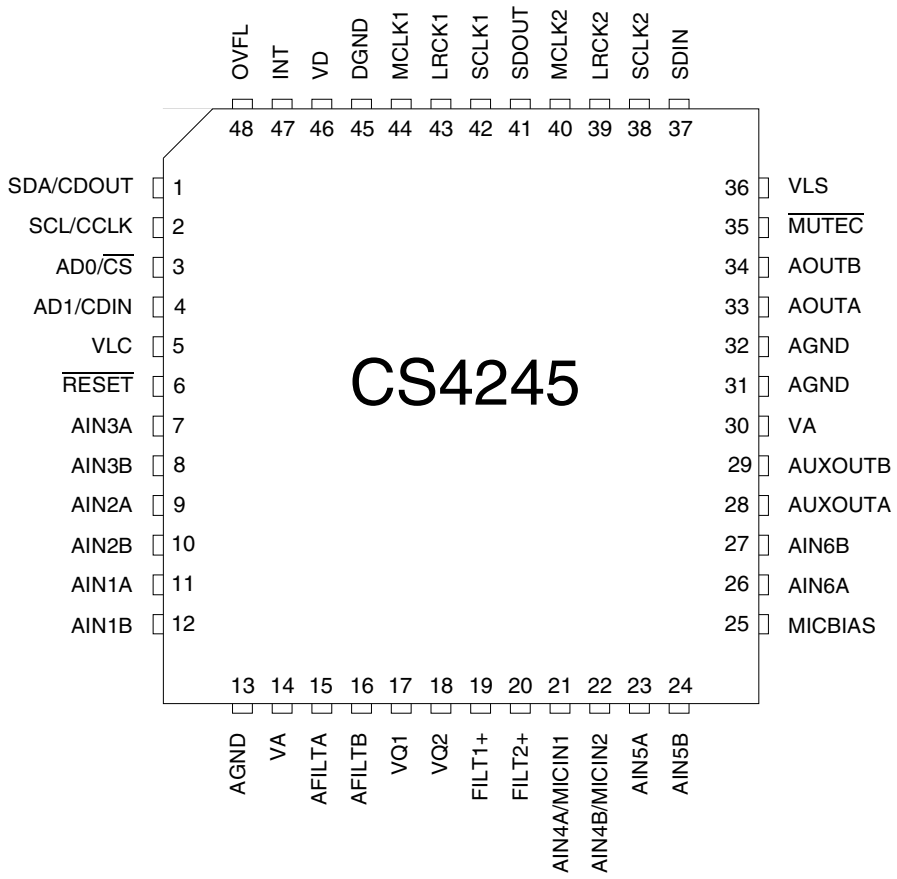
1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA/CDOUT	1	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C mode. CDOUT is the output data line for the control port interface in SPI mode.
SCL/CCLK	2	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
AD0/$\overline{CS}$	3	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C mode; $\overline{CS}$ is the chip select signal for SPI format.
AD1/CDIN	4	**Address Bit 1 (I²C) / Serial Control Data Input (SPI)** *(Input)* - AD1 is a chip address pin in I²C mode; CDIN is the input data line for the control port interface in SPI mode.
VLC	5	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{RESET}$	6	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
AIN3A **AIN3B**	7, 8	**Stereo Analog Input 3** (*Input*) **-** The full scale level is specified in the ADC Analog Characteristics specification table.

AIN2A **AIN2B**	9, 10	**Stereo Analog Input 2** (*Input*) **-** The full scale level is specified in the ADC Analog Characteristics specification table.
AIN1A **AIN1B**	11, 12	**Stereo Analog Input 1** (*Input*) **-** The full scale level is specified in the ADC Analog Characteristics specification table.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
VA	14	**Analog Power** *(Input)* **-** Positive power for the internal analog section.
AFILTA	15	**Antialias Filter Connection** (*Output*) **-** Antialias filter connection for the channel A ADC input.
AFILTB	16	**Antialias Filter Connection** (*Output*) **-** Antialias filter connection for the channel B ADC input.
VQ1	17	**Quiescent Voltage 1** (*Output*) **-** Filter connection for the internal quiescent reference voltage.
VQ2	18	**Quiescent Voltage 2** (*Output*) **-** Filter connection for the internal quiescent reference voltage.
FILT1+	19	**Positive Voltage Reference 1** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
FILT2+	20	**Positive Voltage Reference 2** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
AIN4A/MICIN1 **AIN4B/MICIN2**	21, 22	**Stereo Analog Input 4 / Microphone Input 1 & 2** (*Input*) **-** The full scale level is specified in the ADC Analog Characteristics specification table.
AIN5A **AIN5B**	23, 24	**Stereo Analog Input 5** (*Input*) **-** The full scale level is specified in the ADC Analog Characteristics specification table.
MICBIAS	25	**Microphone Bias Supply** (*Output*) **-** Low noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics specification table.
AIN6A **AIN6B**	26, 27	**Stereo Analog Input 6** (*Input*) **-** The full scale level is specified in the ADC Analog Characteristics specification table.
AUXOUTA **AUXOUTB**	28, 29	**Auxiliary Analog Audio Output** (*Output*) - Analog output from either the DAC, the PGA block, or high impedance. See “Auxiliary Output Source Select (Bits 6:5)” on page 43.
VA	30	**Analog Power** *(Input)* **-** Positive power for the internal analog section.
AGND	31, 32	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
AOUTA **AOUTB**	33, 34	**DAC Analog Audio Output** (*Output*) - The full scale output level is specified in the DAC Analog Characteristics specification table.
$\overline{\text{MUTEC}}	35	**Mute Control** *(Output)* **-** This pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
VLS	36	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
SDIN	37	**Serial Audio Data Input** (*Input*) - Input for two’s complement serial audio data.
SCLK2	38	**Serial Port 2 Serial Bit Clock** *(Input/Output*) **-** Serial bit clock for serial audio interface 2.
LRCK2	39	**Serial Port 2 Left Right Clock** *(Input/Output*) **-** Determines which channel, Left or Right, is currently active on the serial audio input data line.
MCLK2	40	**Master Clock 2** (*Input/Output*) -Optional asynchronous clock source for the DAC’s delta-sigma modulators.
SDOUT	41	**Serial Audio Data Output** (*Output*) **-** Output for two’s complement serial audio data.
SCLK1	42	**Serial Port 1 Serial Bit Clock** *(Input/Output*) **-** Serial bit clock for serial audio interface 1.
LRCK1	43	**Serial Port 1 Left Right Clock** *(Input/Output*) **-** Determines which channel, Left or Right, is currently active on the serial audio output data line.

MCLK1	44	**Master Clock 1** (*Input/Output*) -Clock source for the ADC's delta-sigma modulators. By default, this signal also clocks the DAC's delta-sigma modulators.
DGND	45	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	46	**Digital Power** (*Input*) **-** Positive power for the internal digital section.
INT	47	**Interrupt** (*Output*) **-** Indicates an interrupt condition has occurred.
OVFL	48	**ADC Overflow** (*Output*) **-** Indicates an ADC overflow condition is present.

2. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (AGND = DGND = 0 V; All voltages with respect to ground.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.1	5.0	5.25	V
	Digital	VD	3.1	3.3	5.25	V
	Logic - Serial Port	VLS	1.71	3.3	5.25	V
	Logic - Control Port	VLC	1.71	3.3	5.25	V
Ambient Operating Temperature (Power Applied)		T_A	-10	-	+70	°C

ABSOLUTE MAXIMUM RATINGS (AGND = DGND = 0 V All voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
	Logic - Serial Port	VLS	-0.3	-	+6.0	V
	Logic - Control Port	VLC	-0.3	-	+6.0	V
Input Current	(Note 2)	I_{in}	-	-	±10	mA
Analog Input Voltage		V_{INA}	AGND-0.3	-	VA+0.3	V
Digital Input Voltage	Logic - Serial Port	V_{IND-S}	-0.3	-	VLS+0.3	V
	Logic - Control Port	V_{IND-C}	-0.3	-	VLC+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-20	-	+85	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

DAC ANALOG CHARACTERISTICS (Full-Scale Output Sine Wave, 997 Hz; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 1), Fs = 48/96/192 kHz. Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.) Synchronous mode.

Parameter		Symbol	All Speed Modes Min	Typ	Max	Unit
Dynamic Performance for VA = 5 V						
Dynamic Range	(Note 3)					
18 to 24-Bit	unweighted		96	102	-	dB
	A-Weighted		99	105	-	dB
16-Bit	unweighted		87	93	-	dB
	A-Weighted		90	96	-	dB
Total Harmonic Distortion + Noise	(Note 3)	THD+N				
18 to 24-Bit	0 dB		-	-95	-89	dB
	-20 dB		-	-82	-76	dB
	-60 dB		-	-42	-36	dB
16-Bit	0 dB		-	-93	-87	dB
	-20 dB		-	-73	-67	dB
	-60 dB		-	-33	-27	dB
Dynamic Performance for VA = 3.3 V						
Dynamic Range	(Note 3)					
18 to 24-Bit	unweighted		93	99	-	dB
	A-Weighted		96	102	-	dB
16-Bit	unweighted		85	90	-	dB
	A-Weighted		88	93	-	dB
Total Harmonic Distortion + Noise	(Note 3)	THD+N				
18 to 24-Bit	0 dB		-	-92	-84	dB
	-20 dB		-	-79	-71	dB
	-60 dB		-	-39	-31	dB
16-Bit	0 dB		-	-90	-82	dB
	-20 dB		-	-70	-62	dB
	-60 dB		-	-30	-22	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	0.25	dB
Gain Drift			-	100	-	ppm/°C
Analog Output						
Full Scale Output Voltage			0.60*VA	0.65*VA	0.70*VA	V_{pp}
DC Current draw from an AOUT pin	(Note 4)	I_{OUT}	-	-	10	µA
AC-Load Resistance	(Note 5)	R_L	3	-	-	kΩ
Load Capacitance	(Note 5)	C_L	-	-	100	pF
Output Impedance		Z_{OUT}	-	100	-	Ω

Note: 3. One-half LSB of triangular PDF dither added to data.

4. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC blocking capacitors.

5. Guaranteed by design. See Figure 2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability. C_L affects the dominant pole of the internal output amp; increasing C_L beyond 100 pF can cause the internal op-amp to become unstable.

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 6,9)		Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response			***Single Speed Mode***			
Passband (Note 6)	to -0.05 dB corner		0	-	.4780	Fs
	to -3 dB corner		0	-	.4996	Fs
Frequency Response 10 Hz to 20 kHz			-.01	-	+.08	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 7)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 8)	Fs = 44.1 kHz		-	-	+.05/-.25	dB
Combined Digital and On-chip Analog Filter Response			***Double Speed Mode***			
Passband (Note 6)	to -0.1 dB corner		0	-	.4650	Fs
	to -3 dB corner		0	-	.4982	Fs
Frequency Response 10 Hz to 20 kHz			-.05	-	+.2	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 7)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Combined Digital and On-chip Analog Filter Response			***Quad Speed Mode***			
Passband (Note 6)	to -0.1 dB corner		0	-	0.397	Fs
	to -3 dB corner		0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz			0	-	+0.00004	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 7)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

Notes: 6. Filter response is guaranteed by design.

7. For Single Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
For Double Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
For Quad Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.

8. De-emphasis is available only in Single Speed Mode.

9. Response is clock dependent and will scale with Fs. Note that the amplitude vs. frequency plots of this data (Figures 21 to 30) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

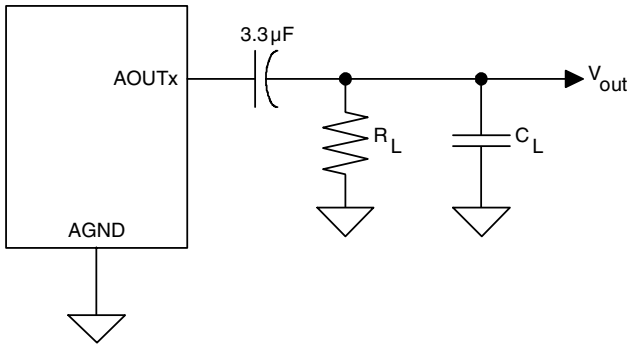


Figure 1. DAC Output Test Load

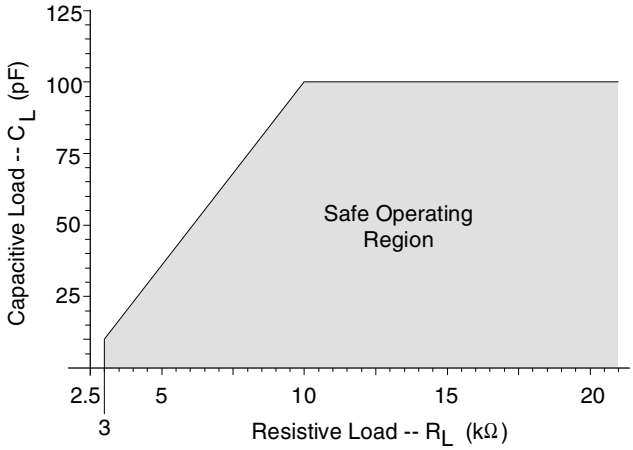


Figure 2. Maximum DAC Loading

ADC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz. Fs = 48/96/192 kHz. Synchronous mode.

Line Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance for VA = 5 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		99	105	-	dB
unweighted		96	102	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	99	-	dB
PGA Setting: +12 dB Gain					
A-weighted		93	99	-	dB
unweighted		90	96	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	93	-	dB
Total Harmonic Distortion + Noise (Note 11)	THD+N				
PGA Setting: -12 dB to +6 dB					
-1 dB		-	-95	-89	dB
-20 dB		-	-82	-	dB
-60 dB		-	-42	-	dB
(Note 12) 40 kHz bandwidth -1 dB		-	-92	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-92	-86	dB
-20 dB		-	-76	-	dB
-60 dB		-	-36	-	dB
(Note 12) 40 kHz bandwidth -1 dB		-	-89	-	dB
Dynamic Performance for VA = 3.3 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		94	102	-	dB
unweighted		91	99	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	96	-	dB
PGA Setting: +12 dB Gain					
A-weighted		90	96	-	dB
unweighted		87	93	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	90	-	dB

Total Harmonic Distortion + Noise (Note 11)		THD+N				
PGA Setting: -12 dB to +6 dB						
-1 dB			-	-92	-86	dB
-20 dB			-	-79	-	dB
-60 dB			-	-39	-	dB
(Note 12)	40 kHz bandwidth	-1 dB		-	-84	-	dB
PGA Setting: +12 dB Gain						
-1 dB			-	-89	-83	dB
-20 dB			-	-73	-	dB
-60 dB			-	-33	-	dB
(Note 12)	40 kHz bandwidth	-1 dB		-	-81	-	dB

Line Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation		-	90	-	dB
Line Level Input Characteristics					
Full-scale Input Voltage		0.53*VA	0.56*VA	0.59*VA	V_{pp}
Input Impedance (Note 10)		6.12	6.8	7.48	kΩ
Maximum Interchannel Input Impedance Mismatch		-	5	-	%

Line Level and Microphone Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error			-	±5	%
Gain Drift		-	±100	-	ppm/°C
Programmable Gain Characteristics					
Gain Step Size		-	0.5	-	dB
Absolute Gain Step Error		-	-	0.4	dB

10. Valid for the selected input pair.

ADC ANALOG CHARACTERISTICS (cont)

Microphone Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance for VA = 5 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 11)	THD+N				
PGA Setting: -12 dB to 0 dB					
-1 dB		-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Dynamic Performance for VA = 3.3 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 11)	THD+N				
PGA Setting: -12 dB to 0 dB					
-1 dB		-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Interchannel Isolation		-	30	-	dB
Microphone Level Input Characteristics					
Full-scale Input Voltage		0.013*VA	0.014*VA	0.015*VA	V_{pp}
Input Impedance (Note 13)		-	100	-	kΩ

11. Referred to the typical line level full-scale input voltage
12. Valid for Double and Quad Speed Modes only.
13. Valid when the microphone level inputs are selected.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 14, 16)	Symbol	Min	Typ	Max	Unit
Single Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.035	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Double Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Quad Speed Mode					
Passband (-0.1 dB)		0	-	0.2604	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5000	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
High Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 15)			20	-	Hz
Phase Deviation @ 20Hz (Note 15)		-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time			10^5/Fs		s

Note: 14. Filter response is guaranteed by design.

15. Response shown is for Fs equal to 48 kHz.

16. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 33 to 44) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

AUXILIARY OUTPUT ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): Synchronous mode, Fs = 48/96/192 kHz. Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

VA = 5 V

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance with PGA Output Selected, Line Level Input					
Dynamic Range (Note 18)					
PGA Setting: -12 dB to +6 dB					
A-weighted		99	105	-	dB
unweighted		96	102	-	dB
PGA Setting: +12 dB Gain					
A-weighted		93	99	-	dB
unweighted		90	96	-	dB
Total Harmonic Distortion + Noise (Note 18)	THD+N				
PGA Setting: -12 dB to +12 dB					
-1 dB		-	-80	-74	dB
-20 dB		-	-82	-	dB
-60 dB		-	-42	-	dB
Dynamic Performance with PGA Output Selected, Mic Level Input					
Dynamic Range (Note 18)					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 18)	THD+N				
PGA Setting: -12 dB to 0 dB					
-1 dB		-	-74	-68	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Dynamic Performance with DAC Output Selected					
Dynamic Range (Notes 17, 18)					
18 to 24-Bit A-Weighted		99	105	-	dB
unweighted		96	102	-	dB
16-Bit A-Weighted		90	96	-	dB
unweighted		87	93	-	dB
Total Harmonic Distortion + Noise (Notes 17, 18)	THD+N				
16 to 24-Bit 0 dB		-	-80	-74	dB
-20 dB		-	-82	-	dB
-60 dB		-	-42	-	dB

AUXILIARY OUTPUT ANALOG CHARACTERISTICS (CONT'D)

VA = 3.3 V

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance with PGA Output Selected, Line Level Input					
Dynamic Range (Note 18)					
PGA Setting: -12 dB to +6 dB					
A-weighted		94	102	-	dB
unweighted		91	99	-	dB
PGA Setting: +12 dB Gain					
A-weighted		90	96	-	dB
unweighted		87	93	-	dB
Total Harmonic Distortion + Noise (Note 18)	THD+N				
PGA Setting: -12 dB to +12 dB					
-1 dB		-	-80	-74	dB
-20 dB		-	-82	-	dB
-60 dB		-	-42	-	dB
Dynamic Performance with PGA Output Selected, Mic Level Input					
Dynamic Range (Note 18)					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 18)	THD+N				
PGA Setting: -12 dB to 0 dB					
-1 dB		-	-74	-68	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Dynamic Performance with DAC Output Selected					
Dynamic Range (Notes 17, 18)					
18 to 24-Bit A-Weighted		96	102	-	dB
unweighted		93	99	-	dB
16-Bit A-Weighted		88	93	-	dB
unweighted		85	90	-	dB
Total Harmonic Distortion + Noise (Notes 17, 18)	THD+N				
16 to 24-Bit 0 dB		-	-80	-74	dB
-20 dB		-	-82	-	dB
-60 dB		-	-42	-	dB

Notes: 17. One-half LSB of triangular PDF dither added to data.

18. Referred to the typical AUXOUT Full-Scale Output Voltage.

AUXILIARY OUTPUT ANALOG CHARACTERISTICS (CONT'D)

VA = 5 V or 3.3 V

Parameter	Symbol	Min	Typ	Max	Unit
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-	±5	-	%
Gain Drift		-	±100	-	ppm/°C
Analog Output					
Full-Scale Output Voltage					
PGA Output Selected		-	0.56*VA	VA	V_{pp}
DAC Output Selected		-	0.7*VA	0.75*VA	V_{pp}
Frequency Response 10 Hz to 20 kHz		-0.1dB	-	+0.1dB	dB
Analog In to Analog Out Phase Shift (Note 19)		-	180	-	deg
DC Current draw from an AUXOUT pin	I_{OUT}	-	-	1	µA
AC-Load Resistance	R_L	100	-	-	kΩ
Load Capacitance	C_L	-	-	20	pF
Output Impedance	Z_{OUT}	-	1	-	kΩ

Notes: 19. Valid only when PGA output is selected.

DC ELECTRICAL CHARACTERISTICS (AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz, Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	41	50	mA
(Normal Operation)	VA = 3.3 V	I_A	-	37	45	mA
	VD, VLS, VLC = 5 V	I_D	-	39	47	mA
	VD, VLS, VLC = 3.3 V	I_D	-	23	28	mA
Power Supply Current.	VA = 5 V	I_A	-	0.50	-	mA
(Power-Down Mode) (Note 20).	VLS, VLC, VD=5 V	I_D	-	0.54	-	mA
Power Consumption						
(Normal Operation).	VA, VD, VLS, VLC = 5 V	-	-	400	485	mW
	VA, VD, VLS, VLC = 3.3 V	-	-	198	241	mW
(Power-Down Mode).	VA, VD, VLS, VLC = 5 V	-	-	4.2	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 21)	PSRR	-	60	-	dB
VQ Characteristics						
Quiescent Voltage 1		VQ1	-	0.5 x VA	-	VDC
DC Current from VQ1	(Note 22)	I_{Q1}	-	-	1	µA
VQ1 Output Impedance		Z_{Q1}	-	23	-	kΩ
Quiescent Voltage 2		VQ2	-	0.5 x VA	-	VDC
DC Current from VQ2	(Note 22)	I_{Q2}	-	-	1	µA
VQ2 Output Impedance		Z_{Q2}	-	23	-	kΩ
FILT1+ Nominal Voltage		FILT1+	-	VA	-	VDC
FILT2+ Nominal Voltage		FILT2+	-	VA	-	VDC
Microphone Bias Voltage		MICBIAS	-	0.8 x VA	-	VDC
Current from MICBIAS		I_{MB}	-	-	2	mA

Notes: 20. Power Down Mode is defines as $\overline{\text{RESET}}$ = Low with all clock and data lines held static and no analog input.

21. Valid with the recommended capacitor values on FILT1+, FILT2+, VQ1 and VQ2 as shown in the Typical Connection Diagram.

22. Guaranteed by design. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE CHARACTERISTICS

Parameters (Note 23)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVLS	V
	Control Port	V_{IL}	-	-	0.2xVLC	V
High-Level Output Voltage at I_o=2 mA	Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
	MUTEC	V_{OH}	VA-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	Serial Port	V_{OL}	-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
	MUTEC	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance	(Note 24)		-	-	1	pF
Maximum MUTEC Drive Current			-	3	-	mA
Minimum OVFL Active Time			$\frac{10^6}{\text{LRCK1}}$			µs

Notes: 23. Serial Port signals include: MCLK1, MCLK2, SCLK1, SCLK2, LRCK1, LRCK2, SDIN, SDOUT. Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/CS, AD1/CDIN, RESET, INT, OVFL.

24. Guaranteed by design.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT 1 (Logic '0' = DGND = 0 V; Logic '1' = VL, C_L = 20 pF) (Note 25)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single Speed Mode	Fs	4	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
	Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications						
MCLK1 Input Frequency		f_{mclk}	1.024	-	51.200	MHz
MCLK1 Input Pulse Width High/Low		t_{clkhl}	8	-	-	ns
Master Mode						
LRCK1 Duty Cycle			-	50	-	%
SCLK1 Duty Cycle			-	50	-	%
SCLK1 falling to LRCK1 edge		t_{slr}	-10	-	10	ns
SCLK1 falling to SDOUT valid		t_{sdo}	0	-	32	ns
Slave Mode						
LRCK1 Duty Cycle			40	50	60	%
SCLK1 Period						
	Single Speed Mode	t_{sclkw}	$\frac{10^9}{(128)Fs}$	-	-	ns
	Double Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
	Quad Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
SCLK1 Pulse Width High		t_{sclkh}	30	-	-	ns
SCLK1 Pulse Width Low		t_{sclkl}	48	-	-	ns
SCLK1 falling to LRCK1 edge		t_{slr}	-10	-	10	ns
SCLK1 falling to SDOUT valid		t_{sdo}	0	-	32	ns

25. See figures 3 and 4 on page 22.

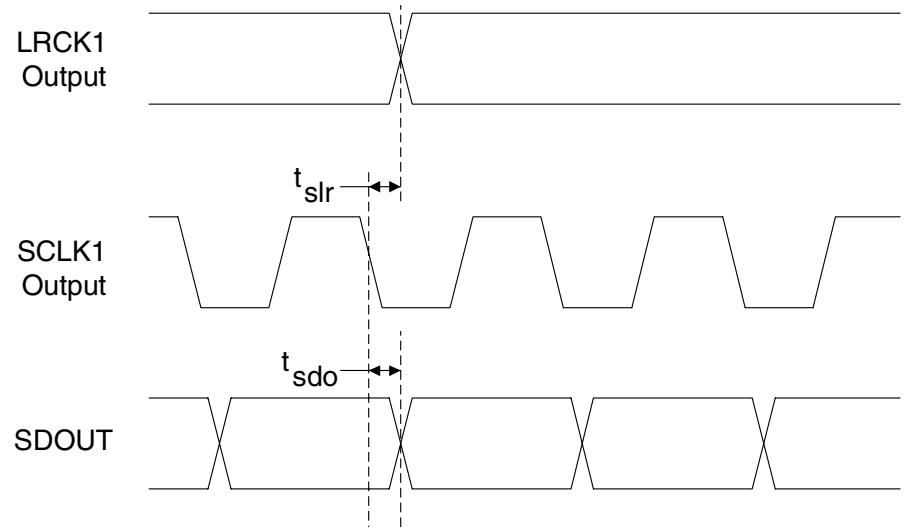


Figure 3. Master Mode Timing - Serial Audio Port 1

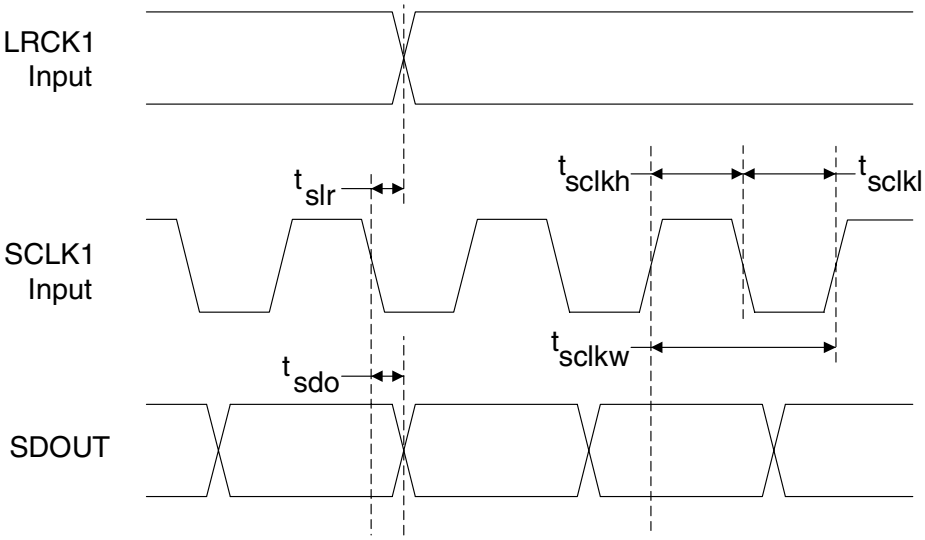


Figure 4. Slave Mode Timing - Serial Audio Port 1

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT 2 (Logic '0' = DGND = 0 V; Logic '1' = VL, C_L = 20 pF) (Note 26)

Parameter	Symbol	Min	Typ	Max	Unit
Sample Rate Single Speed Mode	Fs	4	-	50	kHz
Double Speed Mode	Fs	50	-	100	kHz
Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications					
MCLK2 Input Frequency	f_{mclk}	1.024	-	51.200	MHz
MCLK2 Input Pulse Width High/Low	t_{clkhl}	8	-	-	ns
Master Mode					
LRCK2 Duty Cycle		-	50	-	%
SCLK2 Duty Cycle		-	50	-	%
SCLK2 falling to LRCK edge	t_{slr}	-10	-	10	ns
SDIN valid to SCLK2 rising setup time	t_{sdis}	16	-	-	ns
SCLK2 rising to SDIN hold time	t_{sdih}	20	-	-	ns
Slave Mode					
LRCK2 Duty Cycle		40	50	60	%
SCLK2 Period					
Single Speed Mode	t_{sclkw}	$\frac{10^9}{(128)Fs}$	-	-	ns
Double Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
Quad Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
SCLK2 Pulse Width High	t_{sclkh}	30	-	-	ns
SCLK2 Pulse Width Low	t_{sclkl}	48	-	-	ns
SCLK2 falling to LRCK2 edge	t_{slr}	-10	-	10	ns
SDIN valid to SCLK2 rising setup time	t_{sdis}	16	-	-	ns
SCLK2 rising to SDIN hold time	t_{sdih}	20	-	-	ns

26. See figures 5 and 6 on page 24.

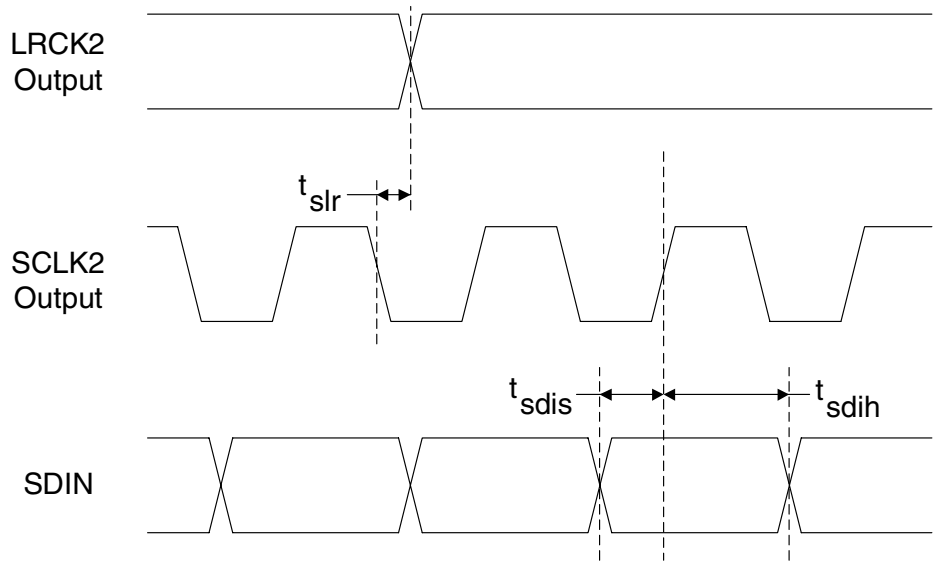


Figure 5. Master Mode Timing - Serial Audio Port 2

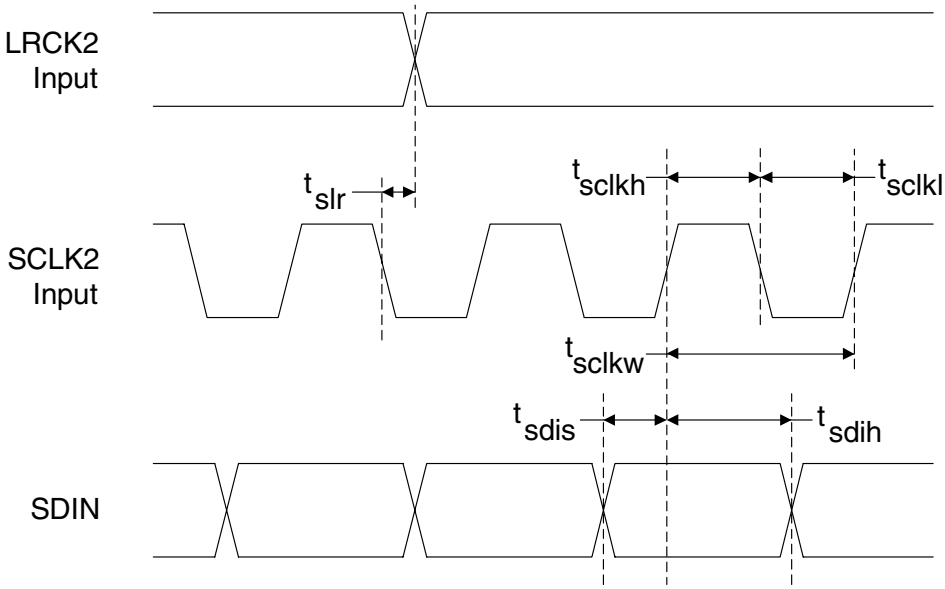


Figure 6. Slave Mode Timing - Serial Audio Port 2

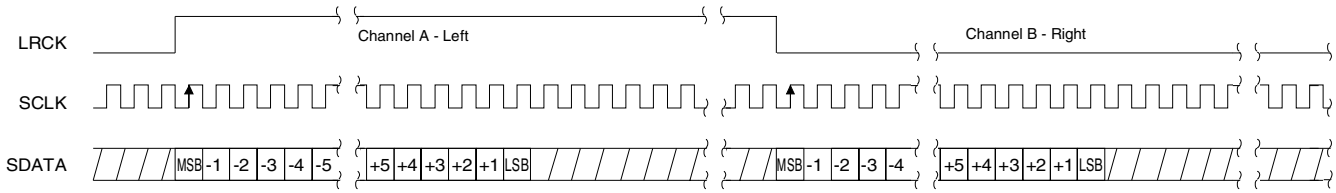


Figure 7. Format 0, Left Justified up to 24-Bit Data

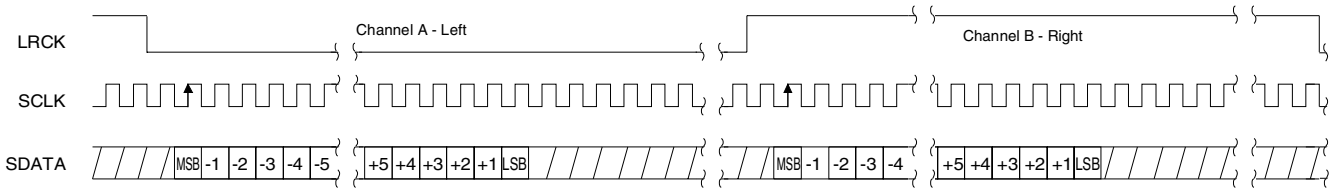


Figure 8. Format 1, I²S up to 24-Bit Data

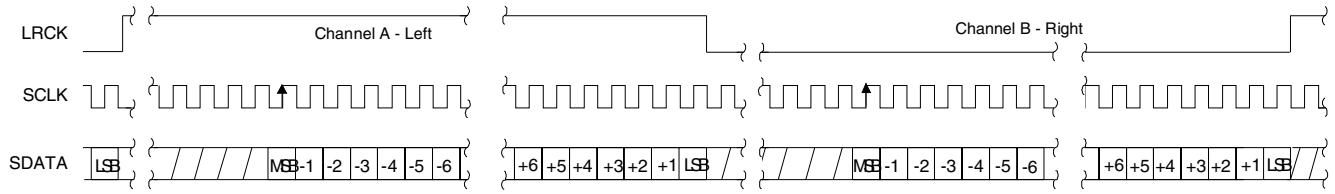


Figure 9. Format 2, Right Justified 16-Bit Data.
Format 3, Right Justified 24-Bit Data.

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 27)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA	(Note 28)	t_{rc}	-	1	µs
Fall Time SCL and SDA	(Note 28)	t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling		t_{ack}	300	1000	ns

Notes: 27. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

28. Guaranteed by design.

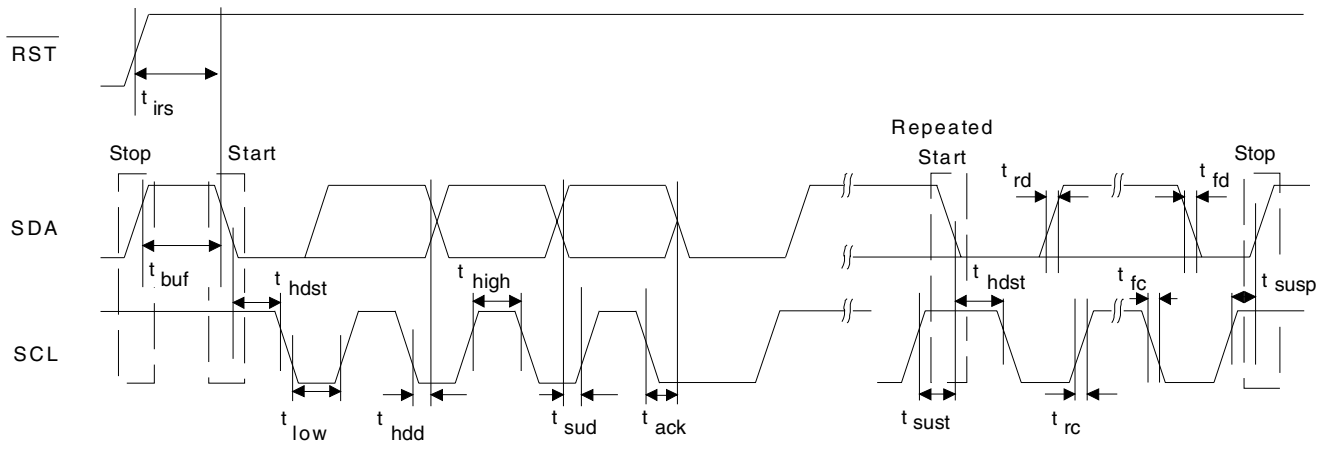


Figure 10. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency		f_{sck}	0	-	6.0	MHz
$\overline{RESET}$ Rising Edge to $\overline{CS}$ Falling.		t_{srs}	500	-	ns	
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 29)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 30)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 30)	t_{f2}	-	-	100	ns

Notes: 29. Data must be held for sufficient time to bridge the transition time of CCLK.

30. For f_{sck} <1 MHz.

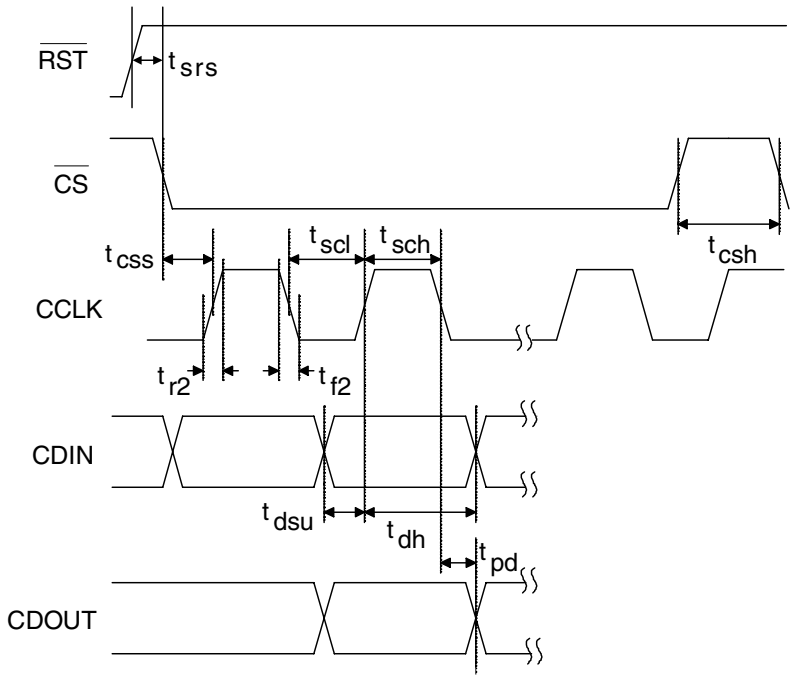


Figure 11. Control Port Timing - SPI Format

3. TYPICAL CONNECTION DIAGRAM

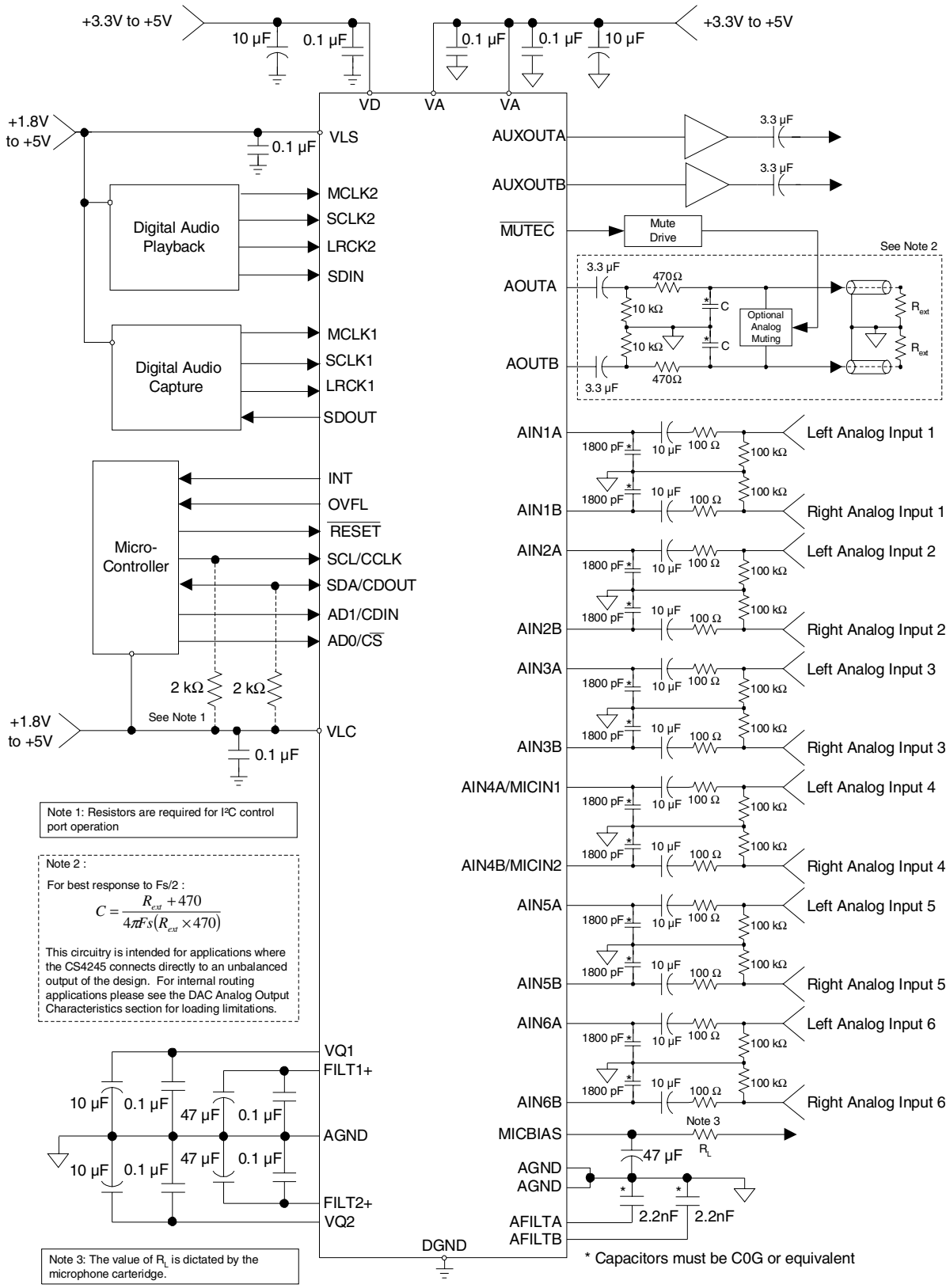


Figure 12. Typical Connection Diagram

4. APPLICATIONS

4.1 Recommended Power-Up Sequence

1) Hold $\overline{\text{RESET}}$ low until the power supply, MCLK1, MCLK2 (if used), LRCK1 and LRCK2 are stable. In this state, the Control Port is reset to its default settings.
2) Bring $\overline{\text{RESET}}$ high. The device will remain in a low power state with the PDN bit set by default. The control port will be accessible.
3) The desired register settings can be loaded while the PDN bit remains set.
4) Clear the PDN bit to initiate the power-up sequence.

4.2 System Clocking

The CS4245 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 1 below.

Mode	Sampling Frequency
Single Speed	4-50 kHz
Double Speed	50-100 kHz
Quad Speed	100-200 kHz

Table 1. Speed Modes

The CS4245 has two serial ports which may be operated synchronously or asynchronously. Serial port 1 consists of the SCLK1 and LRCK1 signals and clocks the serial audio output, SDOUT. Serial port 2 consists of the SCLK2 and LRCK2 signals and clocks the serial audio input, SDIN.

Each serial port may be independently placed into Single, Double, or Quad Speed mode. The serial ports may also be independently placed into Master or Slave mode.

4.2.1 Synchronous / Asynchronous Mode

By default, the CS4245 operates in synchronous mode with both serial ports synchronous to MCLK1. In this mode, the serial ports may operate at different synchronous rates as set by the ADC_FM and DAC_FM bits, and MCLK2 does not need to be provided (the MCLK2 pin may be left unconnected).

If the Asynch bit is set (see “Asynchronous Mode (Bit 0)” on page 43), the CS4245 will operate in asynchronous mode. The serial ports will operate asynchronously with Serial Port 1 clocked from MCLK1 and Serial Port 2 clocked from MCLK2. In this mode, the serial ports may operate at different asynchronous rates.

4.2.2 Master Clock

In asynchronous mode MCLK1/LRCK1 and MCLK2/LRCK2 must maintain an integer ratio. In synchronous mode MCLK1/LRCK1 and MCLK1/LRCK2 must maintain an integer ratio. Some common ratios are shown in Table 2.The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device. The ADC_FM and DAC_FM bits and the MCLK Freq bits (see page 42) configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. Table 2 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)								
	64x	96x	128x	192x	256x	384x	512x	768x	1024x
32	-	-	-	-	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1584
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520
64	-	-	8.1920	12.2880	16.3840	24.5760	32.7680	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	45.1584	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-	-
128	8.1920	12.2880	16.3840	24.5760	32.7680	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	45.1584	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	49.1520	-	-	-	-
Mode	QSM					DSM		SSM	

Table 2. Common Clock Frequencies

4.2.3 Master Mode

As a clock master, LRCK and SCLK will operate as outputs. The two serial ports may be independently placed into Master or Slave mode. Each LRCK and SCLK is internally derived from its respective MCLK with LRCK equal to Fs and SCLK equal to 64 x Fs as shown in Figure 13.

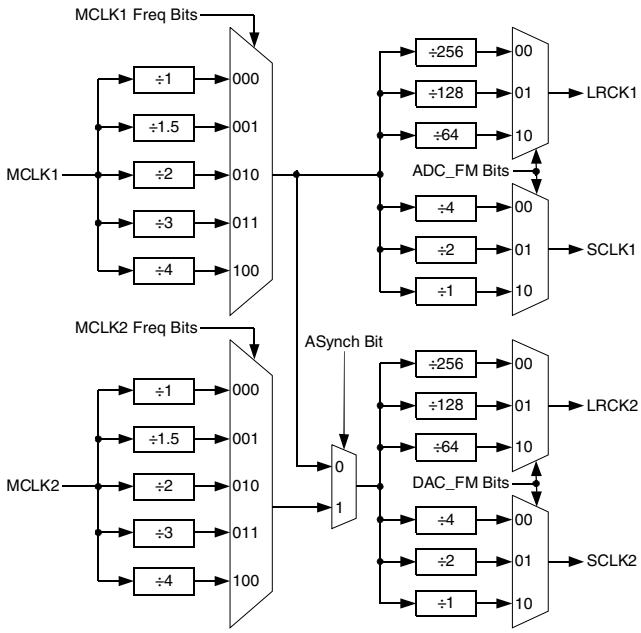


Figure 13. Master Mode Clocking

4.2.4 Slave Mode

In Slave mode, SCLK and LRCK operate as inputs. Each serial port may be independently placed into Slave mode. The Left/Right clock signal must be equal to the sample rate, Fs. If operating in asynchronous mode, LRCK1 must be synchronously derived from MCLK1 and LRCK2 must be synchronously derived from MCLK2. If operating in synchronous mode, LRCK1, and LRCK2 must be synchronously derived from MCLK1. For more information on synchronous and asynchronous modes, see “Synchronous / Asynchronous Mode” on page 29.

For each serial port, the serial bit clock must be equal to 128x, 64x, 48x or 32x Fs depending on the desired speed mode. If operating in asynchronous mode, the serial bit clock SCLK1 must be synchronously derived from MCLK1 and SCLK2 must be synchronously derived from MCLK2. If operating in synchronous mode, SCLK1, and SCLK2 must be synchronously derived from MCLK1. Refer to Table 3 for required serial bit clock to Left/Right clock ratios.

	Single Speed	Double Speed	Quad Speed
SCLK/LRCK Ratio	32x, 48x, 64x, 128x	32x, 48x, 64x	32x, 48x, 64x

Table 3. Slave Mode Serial Bit Clock Ratios

4.3 High Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS4245, a small DC offset may be driven into the A/D converter. The CS4245 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding clicks when switching between devices in a multichannel system.

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPFFreeze bit (see page 42) is set during normal operation, the current value of the DC offset for the each channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1) Running the CS4245 with the high pass filter enabled until the filter settles. See the ADC Digital Filter Characteristics section for filter settling time.
2) Disabling the high pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS4245.

4.4 Analog Input Multiplexer, PGA, and Mic Gain

The CS4245 contains a stereo 6-to-1 analog input multiplexer followed by a programmable gain amplifier (PGA). The input multiplexer can select one of 6 possible stereo analog input sources and route it to the PGA. Analog inputs 4A and 4B are able to insert a +32 dB gain stage before the input multiplexer, allowing them to be used for microphone level signals without the need for any external gain. The PGA stage provides ±12 dB of gain or attenuation in 0.5 dB steps. Figure 14 shows the architecture of the input multiplexer, PGA, and mic gain stages.

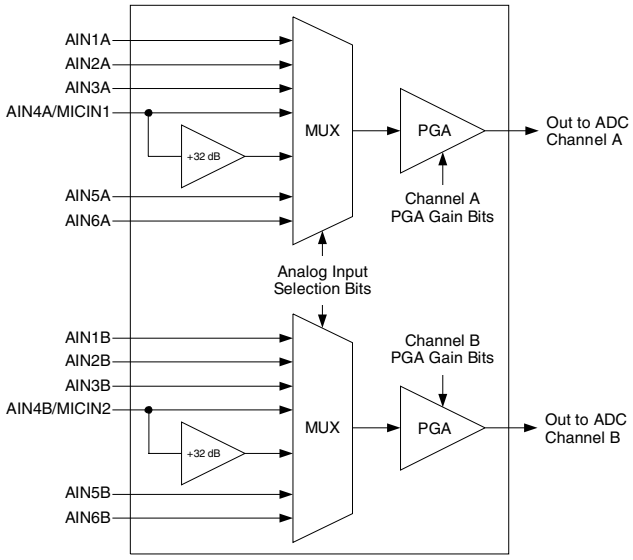


Figure 14. Analog Input Architecture

The “Analog Input Selection (Bits 2:0)” section on page 45 outlines the bit settings necessary to control the input multiplexer and mic gain. “Channel A PGA Control - Address 07h” on page 43 and “Channel B PGA Control - Ad-

dress 08h" on page 44 outlines the register settings necessary to control the PGA. By default, line level input 1 is selected, and the PGA is set to 0 dB.

4.5 Input Connections

The analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are (n × 6.144 MHz) the digital passband frequency, where n=0,1,2,... Refer to the Typical Connection Diagram for the recommended analog input circuit that will attenuate noise energy at 6.144 MHz. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. Any unused analog input pairs should be left unconnected.

4.6 Output Connections

The CS4245 DAC's implement a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is shown in the "DAC Filter Plots" section beginning on page 50. The recommended external analog circuitry is shown in the Typical Connection Diagram.

The CS4245 DAC is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

4.7 Output Transient Control

The CS4245 uses Popguard™ technology to minimize the effects of output transients during power-up and power-down. This technique eliminates the audio transients commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation.

4.7.1 Power-up

When the device is initially powered-up, the audio outputs AOUTA and AOUTB are clamped to VQ2 which is initially low. After the PDN bit is released (set to '0') the DAC outputs begin to ramp with VQ2 towards the nominal quiescent voltage. This ramp takes approximately 200 ms to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ2, effectively blocking the quiescent DC voltage. Audio output will begin after approximately 2000 sample periods.

4.7.2 Power-down

To prevent audio transients at power-down the DC-blocking capacitors must fully discharge before turning off the power. In order to do this either the PDN bit should be set or the device should be reset about 250 ms before removing power. During this time, the voltage on VQ2 and the DAC outputs discharge gradually to GND. If power is removed before this 250 ms time period has passed a transient will occur when the VA supply drops below that of VQ2. There is no minimum time for a power cycle, power may be re-applied at any time.

4.7.3 Serial Interface Clock Changes

When changing the DAC clock ratio or sample rate it is recommended that zero data (or near zero data) be present on SDIN for at least 10 LRCK samples before the change is made. During the clocking change the DAC outputs will always be in a zero data state. If non-zero serial audio input is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to it's zero data state.

4.8 Auxiliary Analog Output

The CS4245 includes an auxiliary analog output through the AUXOUT pins. These pins can be configured to output the analog input to the ADC as selected with the input MUX and gained or attenuated with the PGA, the analog output of the DAC, or alternatively they may be set to high-impedance. See the "Auxiliary Output Source Select (Bits 6:5)" section on page 43 for information on configuring the auxiliary analog output.

The auxiliary analog output can source very little current. As current from the AUXOUT pins increases, distortion will increase. For this reason, a high input impedance buffer must be used on the AUXOUT pins to achieve full performance. Refer to the Auxiliary Output Analog Characteristics table on page 18 for acceptable loading conditions.

4.9 De-Emphasis Filter

The CS4245 includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 15. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. Please see section 6.3.4 for de-emphasis control.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single Speed Mode.

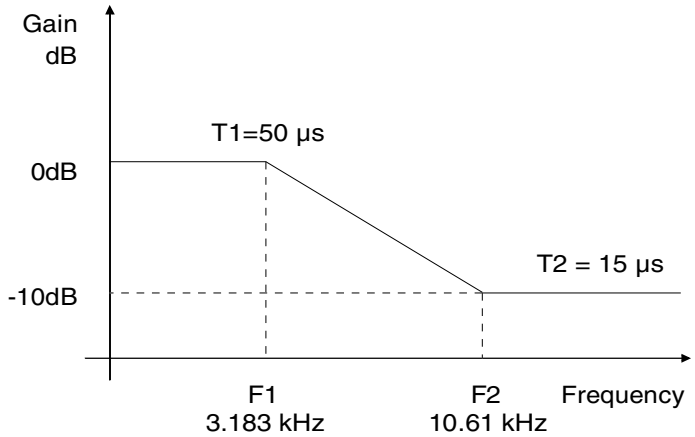


Figure 15. De-Emphasis Curve

4.10 Internal Digital Loopback

The CS4245 supports an internal digital loopback mode in which the output of the ADC is routed to the input of the DAC. This mode may be activated by setting the LOOP bit in the Signal Selection register (06h - See page 43). To use this mode, the ADC and DAC must be operating at the same synchronous sample rate.

When this bit is set, the status of the DAC_DIF[1:0] bits in register 03h will be disregarded by the CS4245. Any changes made to the DAC_DIF[1:0] bits while the LOOP bit is set will have no impact on operation until the LOOP bit is cleared, at which time the Digital Interface Format of the DAC will operate according to the format selected by the DAC_DIF[1:0] bits. While the LOOP bit is set, data will be present on the SDOUT pin in the format selected by the ADC_DIF bit in register 04h.

4.11 Mute Control

The $\overline{\text{MUTEC}}$ pin becomes active during power-up initialization, reset, muting, if the MCLK2 to LRCK2 ratio is incorrect in asynchronous mode or the MCLK1 to LRCK2 ratio is incorrect in synchronous mode, and during power-down. The $\overline{\text{MUTEC}}$ pin is intended to be used as control for an external mute circuit in order to add off-chip mute capability.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle

channel noise/signal-to-noise ratios which are only limited by the external mute circuit. The $\overline{\text{MUTEC}}$ pin is an active-low CMOS driver. See Figure 16 below for a suggested active-low mute circuit.

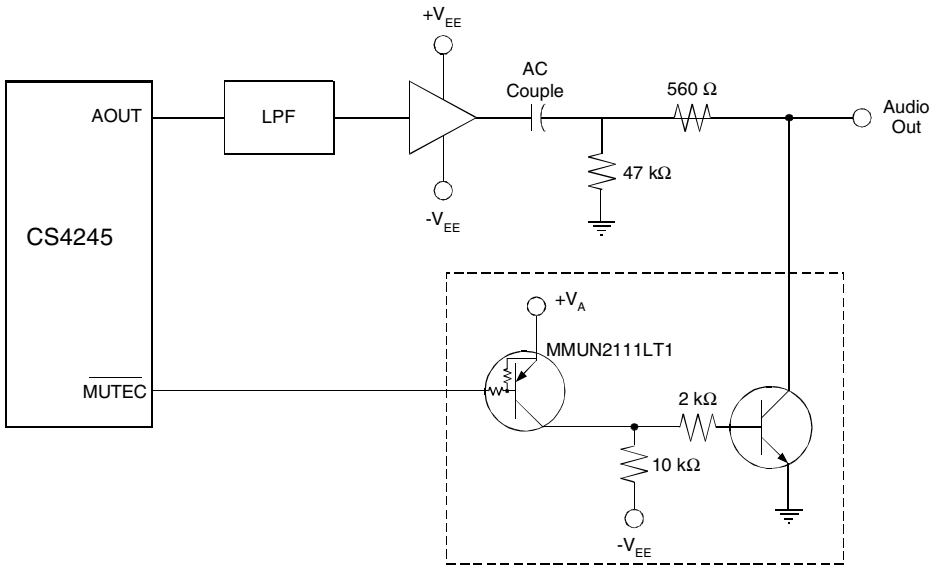


Figure 16. Suggested Active-Low Mute Circuit

4.12 Control Port Description and Timing

The control port is used to access the registers, allowing the CS4245 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I²C, with the CS4245 acting as a slave device. SPI mode is selected if there is a high to low transition on the AD0/$\overline{\text{CS}}$ pin, after the $\overline{\text{RESET}}$ pin has been brought high. I²C mode is selected by connecting the AD0/$\overline{\text{CS}}$ pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

4.12.1 SPI Mode

In SPI mode, $\overline{\text{CS}}$ is the CS4245 chip select signal, CCLK is the control port bit clock (input into the CS4245 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 17 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{\text{CS}}$ low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/$\overline{\text{W}}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{\text{CS}}$ high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{\text{CS}}$ low, send out the chip address and set the read/write bit (R/$\overline{\text{W}}$) high. The next falling edge of CCLK

will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

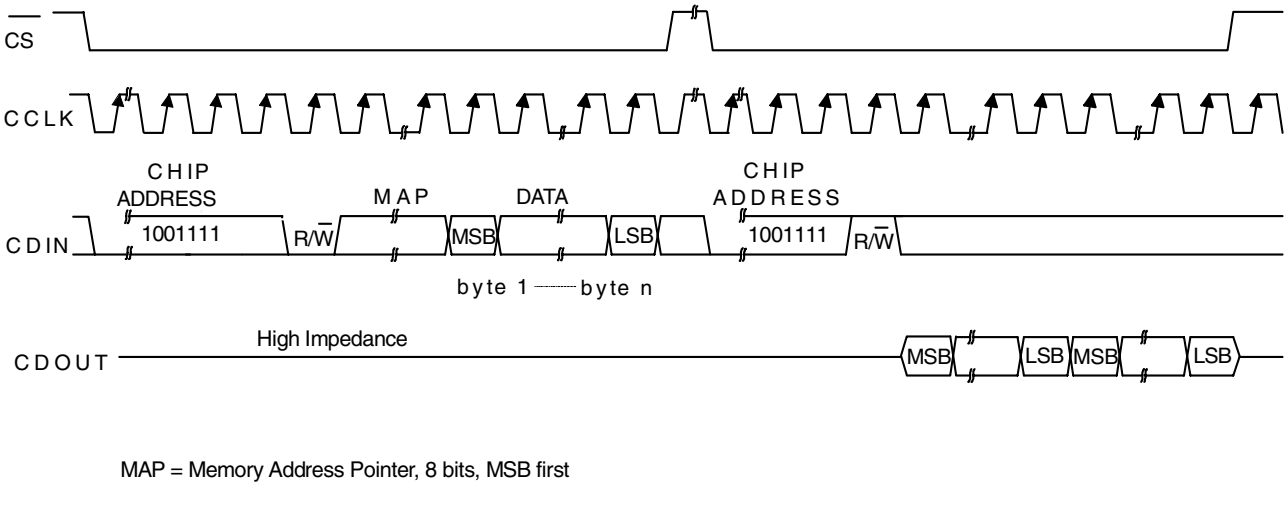


Figure 17. Control Port Timing in SPI Mode

4.12.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS4245 is being reset.

The signal timings for a read and write cycle are shown in Figure 18 and Figure 19. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS4245 after a Start condition consists of a 7 bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS4245, the chip address field, which is the first byte sent to the CS4245, should match 10011 followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS4245 after each input byte is read, and is input to the CS4245 from the microcontroller after each transmitted byte.

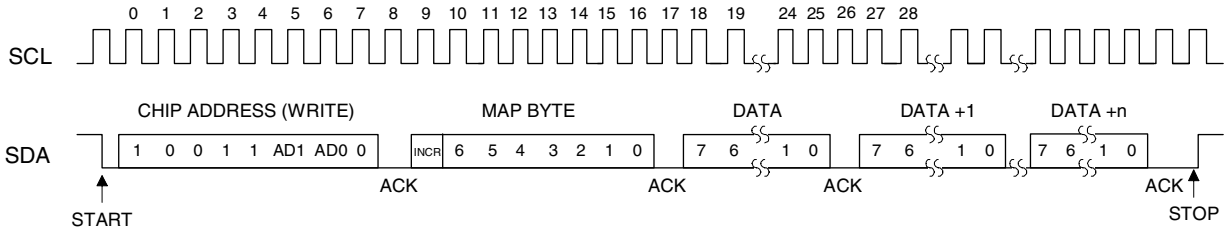


Figure 18. Control Port Timing, I²C Write

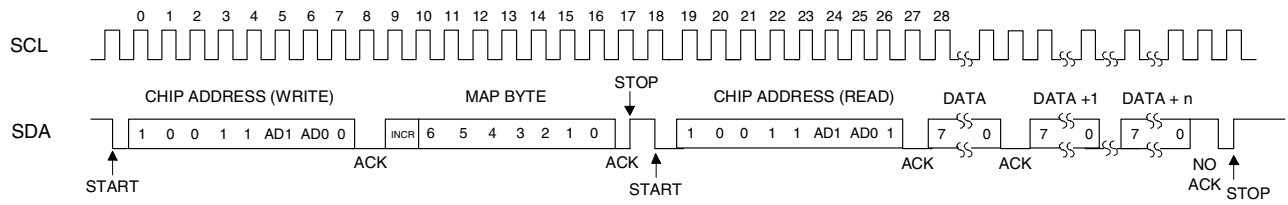


Figure 19. Control Port Timing, I²C Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 19, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 10011xx0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 10011xx1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.13 Interrupts and Overflow

The CS4245 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may function as either an active high CMOS driver or an active low open-drain driver (see “Active High/Low (Bit 0)” on page 46). When configured as active low open-drain, the INT pin has no active pull-up transistor, allowing it to be used for wired-OR hook-ups with multiple peripherals connected to the microcontroller interrupt input pin. In this configuration, an external pull-up resistor must be placed on the INT pin for proper operation.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. See “Interrupt Status - Address 0Dh” on page 46. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

The CS4245 also has a dedicated overflow output. The OVFL pin functions as active low open drain and has no active pull-up transistor, thereby requiring an external pull-up resistor. The OVFL pin outputs an OR of the ADCOverflow and ADCUnderflow conditions available in the Interrupt Status register, however, these conditions do not need to be unmasked for proper operation of the OVFL pin.

4.14 Reset

When $\overline{\text{RESET}}$ is low, the CS4245 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. When $\overline{\text{RESET}}$ is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 0 to the PDN bit in the Power Control register will then cause the part to leave the low power state and begin operation.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the $\overline{\text{RESET}}$ pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the FILT1+ and FILT2+ pins. During this voltage reference ramp delay, both SDOUT and DAC outputs will be automatically muted.

It is recommended that $\overline{\text{RESET}}$ be activated if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.15 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the master clocks and left/right clocks must be the same for all of the CS4245’s in the system. If only one master clock source is needed, one solution is to place one CS4245 in Master Mode, and slave all of the other CS4245’s to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS4245 reset with the inactive edge of master clock. This will ensure that all converters begin sampling on the same clock edge.

4.16 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4245 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 12 shows the recommended power arrangements, with VA connected to a clean supply. VD, which powers the digital filter, may be run from the system logic supply (VLS or VLC) or may be powered from the analog supply (VA) via a resistor. In this case, no additional devices should be powered from VD. Power supply decoupling capacitors should be as near to the CS4245 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT1+, FILT2+, VQ1 and VQ2 pins in order to avoid unwanted coupling into the modulators. The FILT1+, FILT2+, VQ1 and VQ2 decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT1+ and FILT2+ and AGND. The CS4245 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS4245 digital outputs only to CMOS inputs.

5. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Chip ID	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		1	1	0	0	0	0	0	1
02h	Power Control	Freeze	Reserved	Reserved	Reserved	PDN_MIC	PDN_ADC	PDN_DAC	PDN
		0	0	0	0	0	0	0	1
03h	DAC Control 1	DAC_FM1	DAC_FM0	DAC_DIF1	DAC_DIF0	Reserved	MuteDAC	DeEmph	DAC_M/$\overline{S}$
		0	0	0	0	1	0	0	0
04h	ADC Control	ADC_FM1	ADC_FM0	Reserved	ADC_DIF	Reserved	MuteADC	HPFFreeze	ADC_M/$\overline{S}$
		0	0	0	0	0	0	0	0
05h	MCLK Frequency	Reserved	MCLK1 Freq2	MCLK1 Freq1	MCLK1 Freq0	Reserved	MCLK2 Freq2	MCLK2 Freq1	MCLK2 Freq0
		0	0	0	0	0	0	0	0
06h	Signal Selection	Reserved	AOutSel1	AOutSel0	Reserved	Reserved	Reserved	LOOP	ASynch
		0	1	0	0	0	0	0	0
07h	PGA Ch B Gain Control	Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0
		0	0	0	0	0	0	0	0
08h	PGA Ch A Gain Control	Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0
		0	0	0	0	0	0	0	0
09h	Analog Input Control	Reserved	Reserved	Reserved	PGASoft	PGAZero	Sel2	Sel1	Sel0
		0	0	0	1	1	0	0	1
0Ah	DAC Ch A Volume Control	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
		0	0	0	0	0	0	0	0
0Bh	DAC Ch B Volume Control	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
		0	0	0	0	0	0	0	0
0Ch	DAC Control 2	DACSoft	DACZero	InvertDAC	Reserved	Reserved	Reserved	Reserved	Active_H/$\overline{L}$
		1	1	0	0	0	0	0	0
0Dh	Interrupt Status	Reserved	Reserved	Reserved	Reserved	ADCClkErr	DACClkErr	ADCOvfl	ADCUndrfl
		0	0	0	0	0	0	0	0
0Eh	Interrupt Mask	Reserved	Reserved	Reserved	Reserved	ADCClkErrM	DACClkErrM	ADCOvflM	ADCUndrflM
		0	0	0	0	0	0	0	0
0Fh	Interrupt Mode MSB	Reserved	Reserved	Reserved	Reserved	ADCClkErr1	DACClkErr1	ADCOvfl1	ADCUndrfl1
		0	0	0	0	0	0	0	0
10h	Interrupt Mode LSB	Reserved	Reserved	Reserved	Reserved	ADCClkErr0	DACClkErr0	ADCOvfl0	ADCUndrfl0
		0	0	0	0	0	0	0	0

6. REGISTER DESCRIPTION

6.1 Chip ID - Register 01h

B7	B6	B5	B4	B3	B2	B1	B0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

Function:

This register is Read-Only. Bits 7 through 4 are the part number ID which is 1100b (0Ch) and the remaining bits (3 through 0) are for the chip revision.

6.2 Power Control - Address 02h

7	6	5	4	3	2	1	0
Freeze	Reserved	Reserved	Reserved	PDN_MIC	PDN_ADC	PDN_DAC	PDN

6.2.1 Freeze (Bit 7)

Function:

This function allows modifications to be made to certain control port bits without the changes taking effect until the Freeze bit is disabled. To make multiple changes to these bits take effect simultaneously, set the Freeze bit, make all changes, then clear the Freeze bit. The bits affected by the Freeze function are listed in Table 4 below.

Table 4. Freeze-able Bits

Name	Register	Bit(s)
MuteDAC	03h	2
MuteADC	04h	2
Gain[5:0]	07h	5:0
Gain[5:0]	08h	5:0
Vol[7:0]	0Ah	7:0
Vol[7:0]	0Bh	7:0

6.2.2 Power Down MIC (Bit 3)

Function:

The microphone preamplifier block will enter a low-power state whenever this bit is set.

6.2.3 Power Down ADC (Bit 2)

Function:

The ADC pair will remain in a reset state whenever this bit is set.

6.2.4 Power Down DAC (Bit 1)

Function:

The DAC pair will remain in a reset state whenever this bit is set.

6.2.5 Power Down Device (Bit 0)

Function:

The device will enter a low-power state whenever this bit is set. The power-down bit is set by default and must be cleared before normal operation can occur. The contents of the control registers are retained when the device is in power-down.

6.3 DAC Control - Address 03h

7	6	5	4	3	2	1	0
DAC_FM1	DAC_FM0	DAC_DIF1	DAC_DIF0	Reserved	MuteDAC	DeEmph	DAC_M/$\overline{S}$

6.3.1 DAC Functional Mode (Bits 7:6)

Function:

Selects the required range of input sample rates.

Table 5. Functional Mode Selection

DAC_FM1	DAC_FM0	Mode
0	0	Single-Speed Mode: 4 to 50 kHz sample rates
0	1	Double-Speed Mode: 50 to 100 kHz sample rates
1	0	Quad-Speed Mode: 100 to 200 kHz sample rates
1	1	Reserved

6.3.2 DAC Digital Interface Format (Bits 5:4)

Function:

The required relationship between LRCK, SCLK and SDIN for the DAC is defined by the DAC Digital Interface Format and the options are detailed in Table 6 and Figures 7-9.

Table 6. DAC Digital Interface Formats

DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	0	Left Justified, up to 24-bit data (default)	0	7
0	1	I^2S, up to 24-bit data	1	8
1	0	Right Justified, 16-bit Data	2	9
1	1	Right Justified, 24-bit Data	3	9

6.3.3 Mute DAC (Bit 2)

Function:

The DAC outputs will mute and the MUTEC pin will become active when this bit is set. Though this bit is active high, it should be noted that the MUTEC pin is active low. The common mode voltage on the outputs will be retained when this bit is set. The muting function is effected, similar to attenuation changes, by the DACSoft and DACZero bits in the DAC Control 2 register.

6.3.4 De-Emphasis Control (Bit 1)

Function:

The standard 50/15 µs digital de-emphasis filter response, Figure 20, may be implemented for a sample rate of 44.1 kHz when the DeEmph bit is configured as shown in Table 7 below. NOTE: De-emphasis is available only in Single-Speed Mode.

Table 7. De-Emphasis Control

DeEmph	Description
0	Disabled (default)
1	44.1 kHz de-emphasis

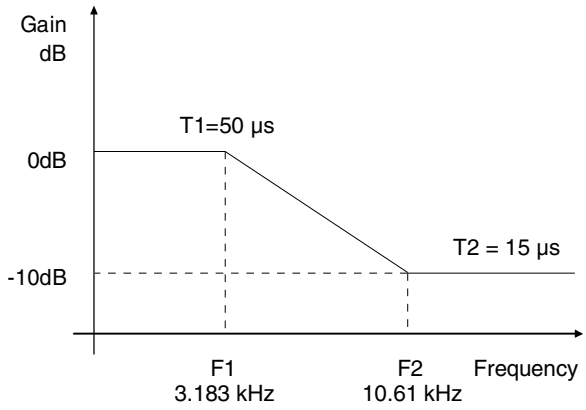


Figure 20. De-Emphasis Curve

6.3.5 DAC Master / Slave Mode (Bit 0)

Function:

This bit selects either master or slave operation for serial audio port 2. Setting this bit will select master mode, while clearing this bit will select slave mode.

6.4 ADC Control - Address 04h

7	6	5	4	3	2	1	0
ADC_FM1	ADC_FM0	Reserved	ADC_DIF	Reserved	MuteADC	HPFFreeze	ADC_M/$\overline{S}$

6.4.1 ADC Functional Mode (Bits 7:6)

Function:

Selects the required range of output sample rates.

Table 8. Functional Mode Selection

ADC_FM1	ADC_FM0	Mode
0	0	Single-Speed Mode: 4 to 50 kHz sample rates
0	1	Double-Speed Mode: 50 to 100 kHz sample rates
1	0	Quad-Speed Mode: 100 to 200 kHz sample rates
1	1	Reserved

6.4.2 ADC Digital Interface Format (Bit 4)

Function:

The required relationship between LRCK1, SCLK1 and SDOUT is defined by the ADC Digital Interface Format bit. The options are detailed in Table 9 and may be seen in Figure 7 and 8.

Table 9. ADC Digital Interface Formats

ADC_DIF	Description	Format	Figure
0	Left Justified, up to 24-bit data (default)	0	7
1	I^2S, up to 24-bit data	1	8

6.4.3 Mute ADC (Bit 2)

Function:

When this bit is set, the serial audio output of the both ADC channels will be muted.

6.4.4 ADC High Pass Filter Freeze (Bit 1)

Function:

When this bit is set, the internal high-pass filter will be disabled.The current DC offset value will be frozen and continue to be subtracted from the conversion result. See "High Pass Filter and DC Offset Calibration" on page 31.

6.4.5 ADC Master / Slave Mode (Bit 0)

Function:

This bit selects either master or slave operation for serial audio port 1. Setting this bit will select master mode, while clearing this bit will select slave mode.

6.5 MCLK Frequency - Address 05h

7	6	5	4	3	2	1	0
Reserved	MCLK1 Freq2	MCLK1 Freq1	MCLK1 Freq0	Reserved	MCLK2 Freq2	MCLK2 Freq1	MCLK2 Freq0

6.5.1 Master Clock 1 Frequency (Bits 6:4)

Function:

Sets the frequency of the supplied MCLK1 signal. See Table 10 below for the appropriate settings.

Table 10. MCLK1 Frequency

MCLK1 Divider	MCLK1 Freq2	MCLK1 Freq1	MCLK1 Freq0
÷ 1	0	0	0
÷ 1.5	0	0	1
÷ 2	0	1	0
÷ 3	0	1	1
÷ 4	1	0	0
Reserved	1	0	1
Reserved	1	1	x

6.5.2 Master Clock 2 Frequency (Bits 2:0)

Function:

Sets the frequency of the supplied MCLK2 signal. See Table 11 below for the appropriate settings.

Table 11. MCLK2 Frequency

MCLK2 Divider	MCLK2 Freq2	MCLK2 Freq1	MCLK2 Freq0
÷ 1	0	0	0
÷ 1.5	0	0	1
÷ 2	0	1	0
÷ 3	0	1	1
÷ 4	1	0	0
Reserved	1	0	1
Reserved	1	1	x

6.6 Signal Selection - Address 06h

7	6	5	4	3	2	1	0
Reserved	AOutSel1	AOutSel0	Reserved	Reserved	Reserved	LOOP	ASynch

6.6.1 Auxiliary Output Source Select (Bits 6:5)

Function:

These bits are used to select the analog output source. Please refer to Table 12 below.

Table 12. Auxiliary Output Source Selection

AOutSel1	AOutSel0	Auxiliary Output Source
0	0	High Impedance
0	1	DAC Output
1	0	PGA Output
1	1	Reserved

6.6.2 Digital Loopback (Bit 1)

Function:

When this bit is set, an internal digital loopback from the ADC to the DAC will be enabled. Please refer to “Internal Digital Loopback” on page 33.

6.6.3 Asynchronous Mode (Bit 0)

Function:

When this bit is set, the DAC and ADC may be operated at independent an asynchronous sample rates derived from MCLK1 and MCLK2. When this bit is cleared, the DAC and ADC must operate at synchronous sample rates derived from MCLK1.

6.7 Channel A PGA Control - Address 07h

7	6	5	4	3	2	1	0
Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0

6.7.1 Channel A PGA Gain (Bits 5:0)

Function:

See “Channel B PGA Gain (Bits 5:0)” on page 44.

6.8 Channel B PGA Control - Address 08h

7	6	5	4	3	2	1	0
Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0

6.8.1 Channel B PGA Gain (Bits 5:0)

Function:

Sets the gain or attenuation for the ADC input PGA stage. The gain may be adjusted from -12 dB to +12 dB in 0.5 dB steps. The gain bits are in two's complement with the Gain0 bit set for a 0.5 dB step. Register settings outside of the ±12 dB range are reserved and must not be used. See Table 13 for example settings.

Table 13. Example Gain and Attenuation Settings

Gain[5:0]	Setting
101000	-12 dB
000000	0 dB
011000	+12 dB

6.9 ADC Input Control - Address 09h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	PGASoft	PGAZero	Sel2	Sel1	Sel0

6.9.1 PGA Soft Ramp or Zero Cross Enable (Bits 4:3)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 14 on page 45.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 14 on page 45.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 14 on page 45.

Table 14. PGA Soft Cross or Zero Cross Mode Selection

PGASoft	PGAZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

6.9.2 Analog Input Selection (Bits 2:0)

Function:

These bits are used to select the input source for the PGA and ADC. Please see Table 15 below.

Table 15. Analog Input Multiplexer Selection

Sel2	Sel1	Sel0	PGA/ADC Input
0	0	0	Microphone Level Inputs (+32 dB Gain Enabled)
0	0	1	Line Level Input Pair 1
0	1	0	Line Level Input Pair 2
0	1	1	Line Level Input Pair 3
1	0	0	Line Level Input Pair 4
1	0	1	Line Level Input Pair 5
1	1	0	Line Level Input Pair 6
1	1	1	Reserved

6.10 DAC Channel A Volume Control - Address 0Ah

See 6.11 DAC Channel B Volume Control - Address 0Bh

6.11 DAC Channel B Volume Control - Address 0Bh

7	6	5	4	3	2	1	0
Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0

6.11.1 Volume Control (Bits 7:0)

Function:

The digital volume control allows the user to attenuate the signal in 0.5 dB increments from 0 to -127 dB. The Vol0 bit activates a 0.5 dB attenuation when set, and no attenuation when cleared. The Vol[7:1] bits activate attenuation equal to their decimal equivalent (in dB). Example volume settings are decoded as shown in Table Table 16. The volume changes are implemented as dictated by the DACSoft and DACZeroCross bits in the DAC Control 2 register (see section 6.12.1).

Table 16. Digital Volume Control Example Settings

Binary Code	Volume Setting
00000000	0 dB
00000001	-0.5 dB
00101000	-20 dB
00101001	-20.5 dB
11111110	-127 dB
11111111	-127.5 dB

6.12 DAC Control 2 - Address 0Ch

7	6	5	4	3	2	1	0
DACSoft	DACZero	InvertDAC	Reserved	Reserved	Reserved	Reserved	Active_H/$\overline{L}$

6.12.1 DAC Soft Ramp or Zero Cross Enable (Bits 7:6)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 17 on page 46.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 17 on page 46.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 17 on page 46.

Table 17. DAC Soft Cross or Zero Cross Mode Selection

DACSoft	DACZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

6.12.2 Invert DAC Output (Bit 5)

Function:

When this bit is set, the output of the DAC will be inverted.

6.12.3 Active High/$\overline{\text{Low}}$ (Bit 0)

Function:

When this bit is set, the INT pin will function as an active high CMOS driver.

When this bit is cleared, the INT pin will function as an active low open drain driver and will require an external pull-up resistor for proper operation.

6.13 Interrupt Status - Address 0Dh

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ADCClkErr	DACClkErr	ADCOvfl	ADCUndrfl

For all bits in this register, a ‘1’ means the associated interrupt condition has occurred at least once since the register was last read. A ‘0’ means the associated interrupt condition has NOT occurred

since the last reading of the register. Status bits that are masked off in the associated mask register will always be '0' in this register. This register defaults to 00h.

6.13.1 ADC Clock Error (Bit 3)

Function:

Indicates the occurrence of an ADC clock error condition.

6.13.2 DAC Clock Error (Bit 2)

Function:

Indicates the occurrence of a DAC clock error condition.

6.13.3 ADC Overflow (Bit 1)

Function:

Indicates the occurrence of an ADC overflow condition.

6.13.4 ADC Underflow (Bit 0)

Function:

Indicates the occurrence of an ADC underflow condition.

6.14 Interrupt Mask - Address 0Eh

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ADCClkErrM	DACClkErrM	ADCOvflM	ADCUndrflM

Function:

The bits of this register serve as a mask for the Status sources found in the register "Interrupt Status - Address 0Dh" on page 46. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in the Status register.

6.15 Interrupt Mode MSB - Address 0Fh

6.16 Interrupt Mode LSB - Address 10h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ADCClkErr1	DACClkErr1	ADCOvfl1	ADCUndrfl1
Reserved	Reserved	Reserved	Reserved	ADCClkErr0	DACClkErr0	ADCOvfl0	ADCUndrfl0

Function:

The two Interrupt Mode registers form a 2-bit code for each Interrupt Status register function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT pin remains active during the interrupt condition.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

7. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

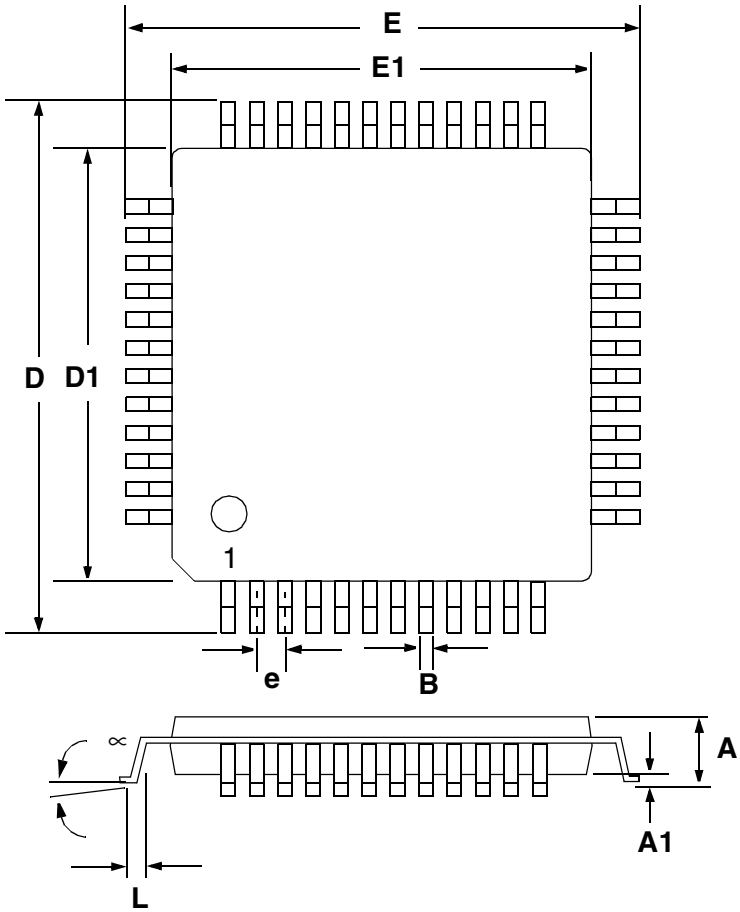
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

8. PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm *Controlling dimension is mm. *JEDEC Designation: MS022

9. THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance (Note 31)	48-LQFP	θ_{JA}	-	48	-	°C/Watt
		θ_{JC}	-	15	-	°C/Watt
Allowable Junction Temperature			-	-	125	°C

Notes: 31. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

APPENDIX A: DAC FILTER PLOTS

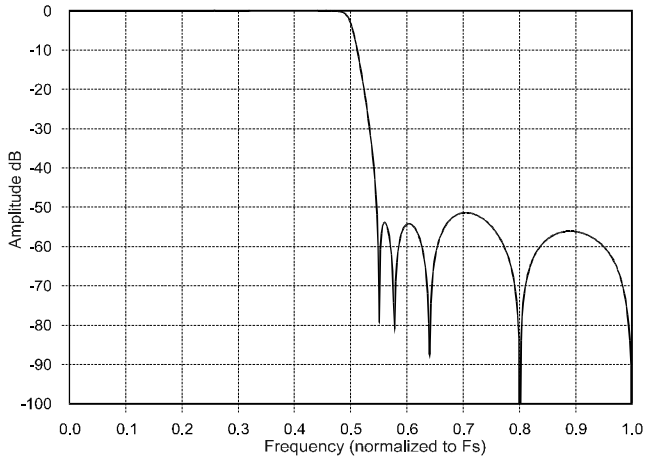


Figure 21. DAC Single Speed Stopband Rejection

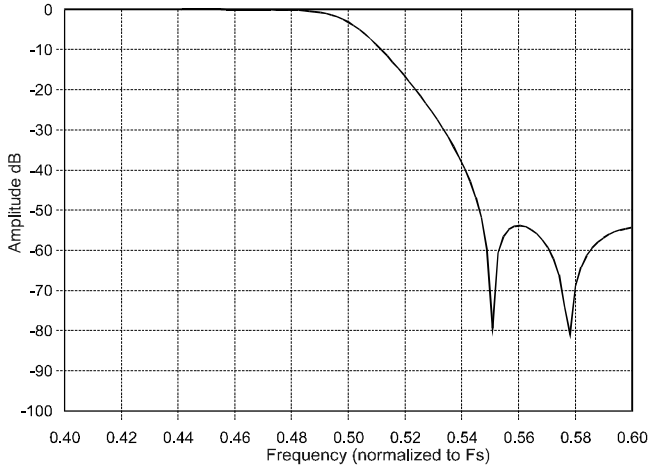


Figure 22. DAC Single Speed Transition Band

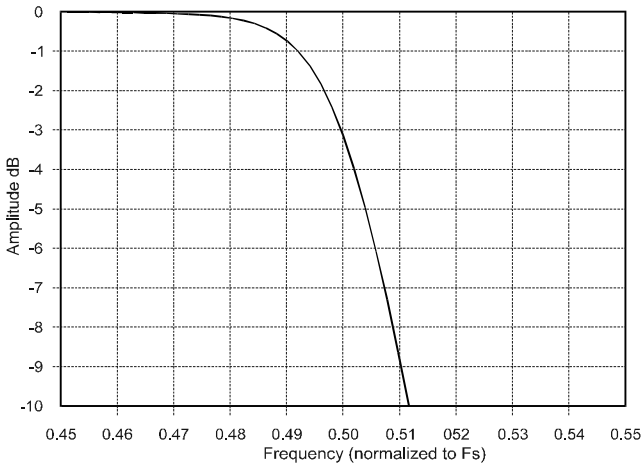


Figure 23. DAC Single Speed Transition Band

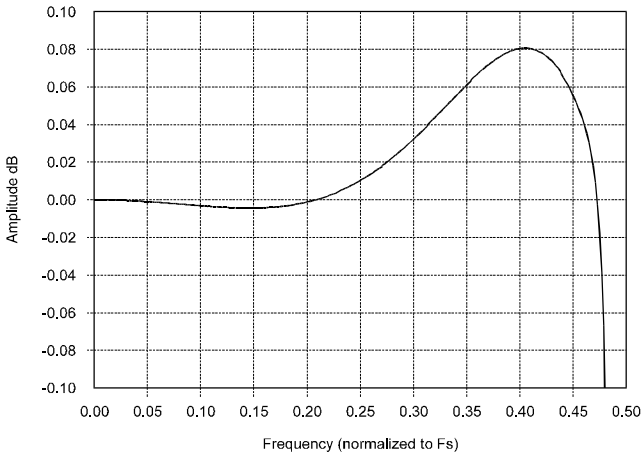


Figure 24. DAC Single Speed Passband Ripple

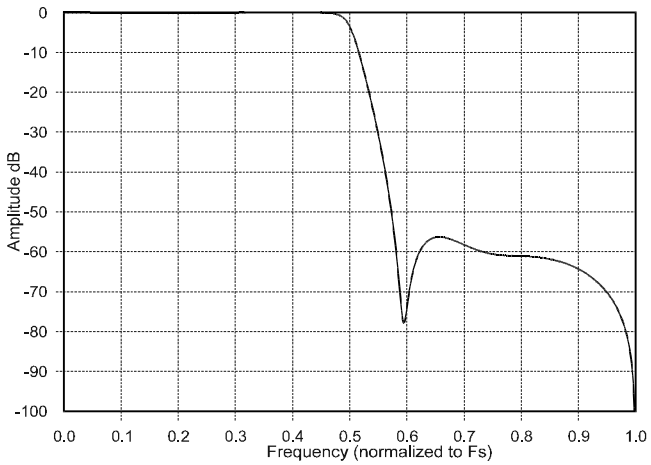


Figure 25. DAC Double Speed Stopband Rejection

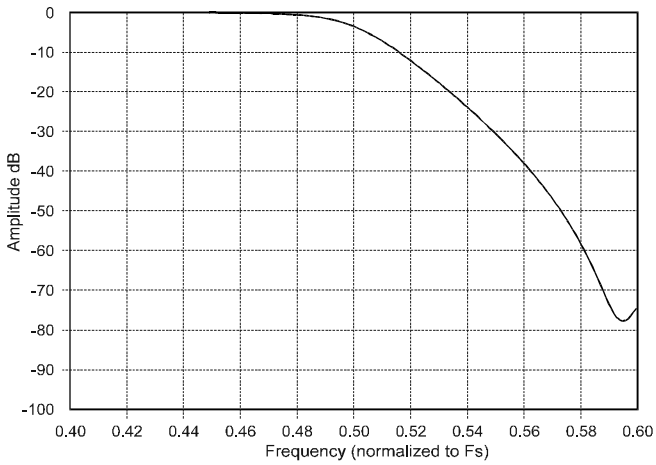


Figure 26. DAC Double Speed Transition Band

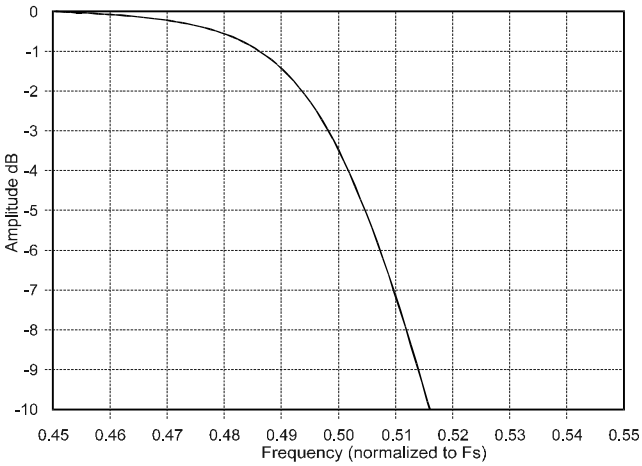


Figure 27. DAC Double Speed Transition Band

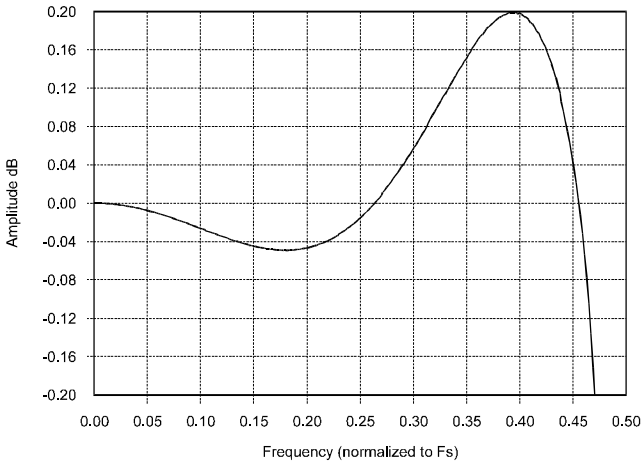


Figure 28. DAC Double Speed Passband Ripple

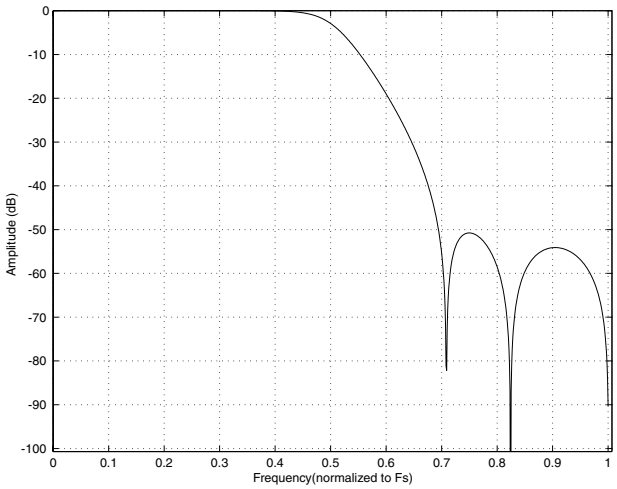


Figure 29. DAC Quad Speed Stopband Rejection

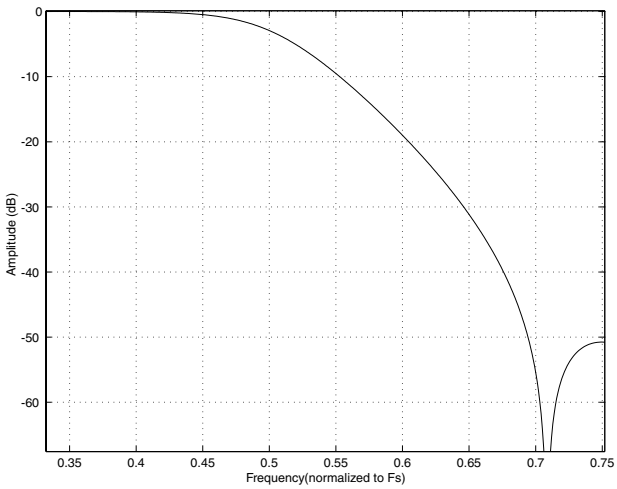


Figure 30. DAC Quad Speed Transition Band

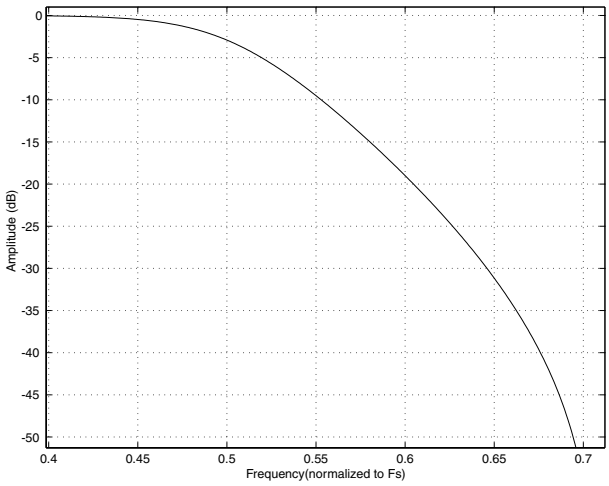


Figure 31. DAC Quad Speed Transition Band

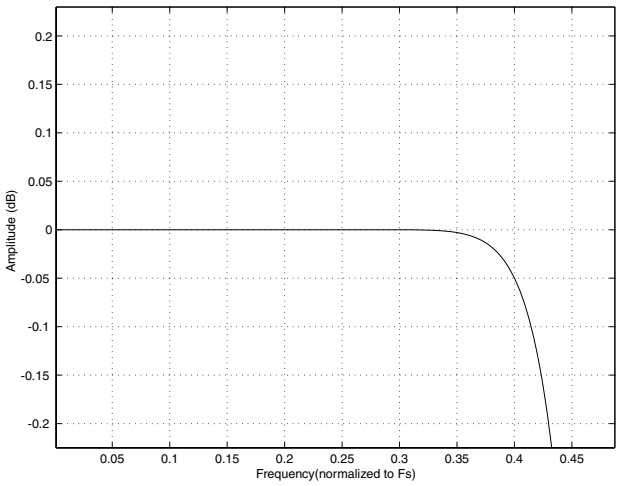


Figure 32. DAC Quad Speed Passband Ripple

APPENDIX B: ADC FILTER PLOTS

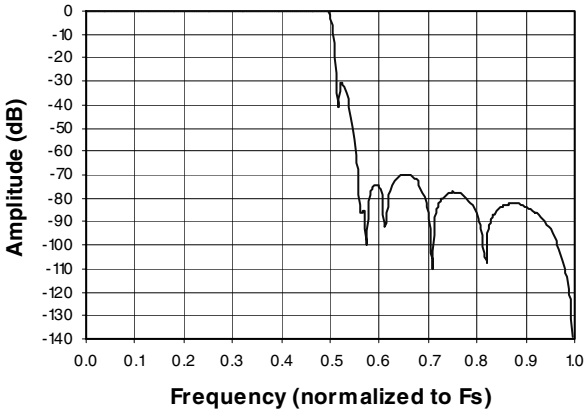


Figure 33. ADC Single Speed Stopband Rejection

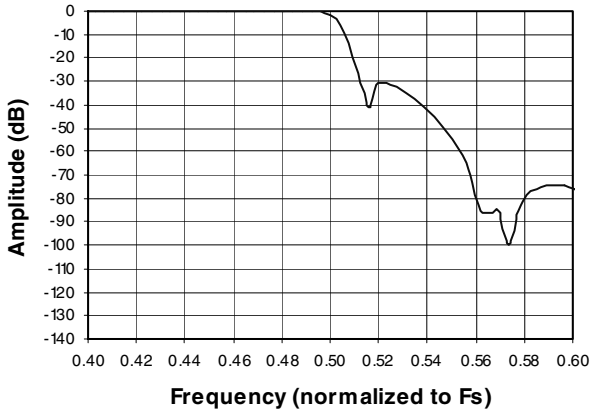


Figure 34. ADC Single Speed Stopband Rejection

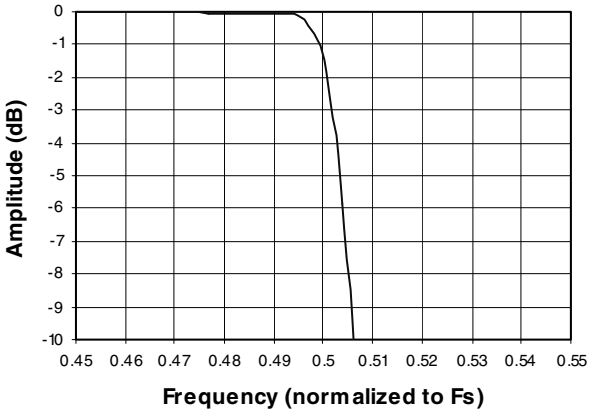


Figure 35. ADC Single Speed Transition Band (Detail)

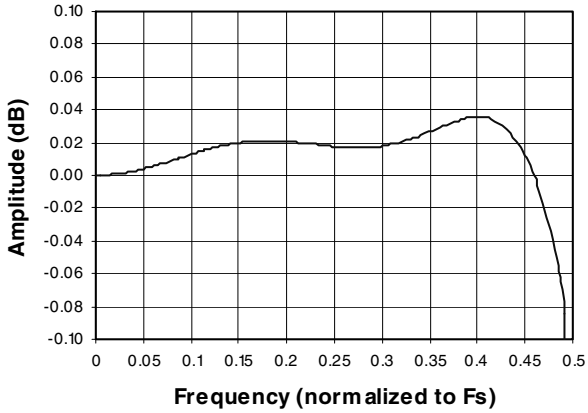


Figure 36. ADC Single Speed Passband Ripple

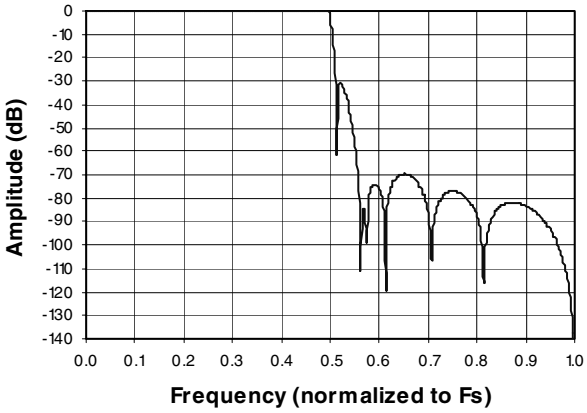


Figure 37. ADC Double Speed Stopband Rejection

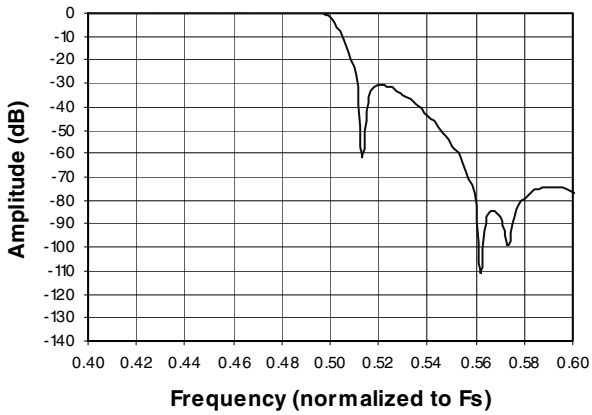


Figure 38. ADC Double Speed Stopband Rejection

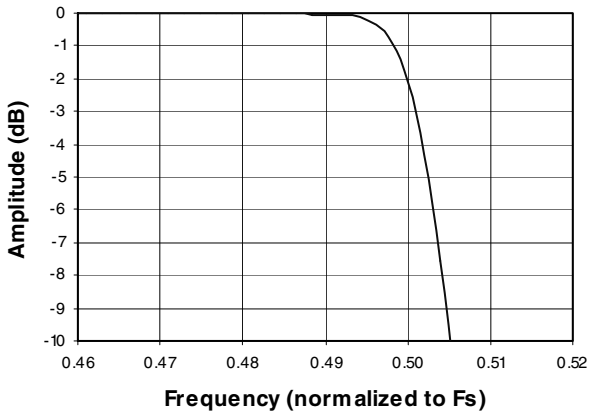


Figure 39. ADC Double Speed Transition Band (Detail)

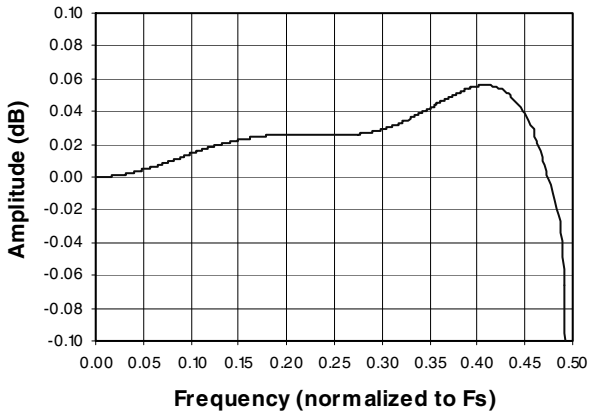


Figure 40. ADC Double Speed Passband Ripple

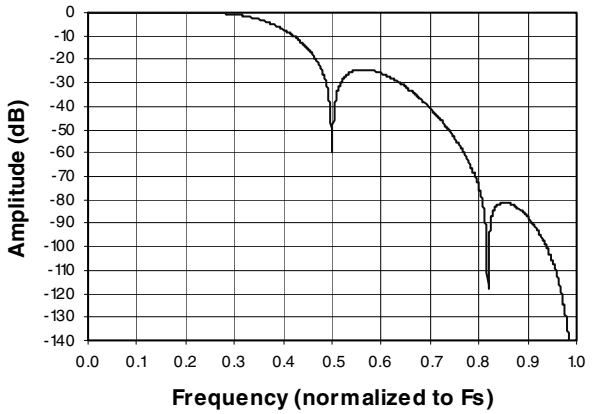


Figure 41. ADC Quad Speed Stopband Rejection

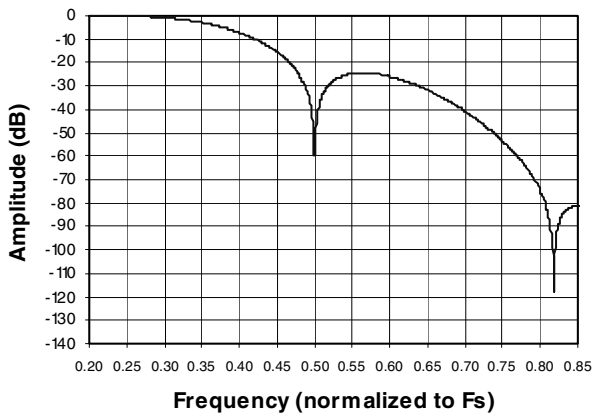


Figure 42. ADC Quad Speed Stopband Rejection

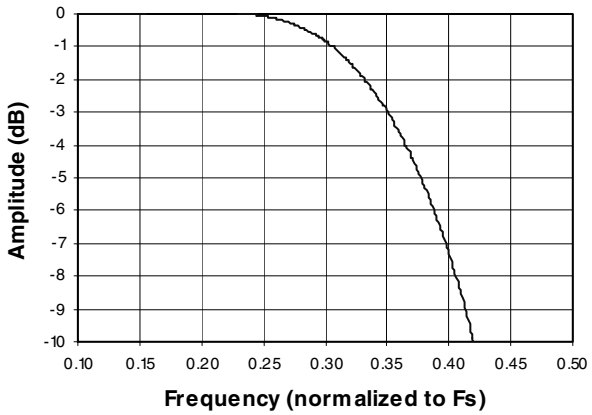


Figure 43. ADC Quad Speed Transition Band (Detail)

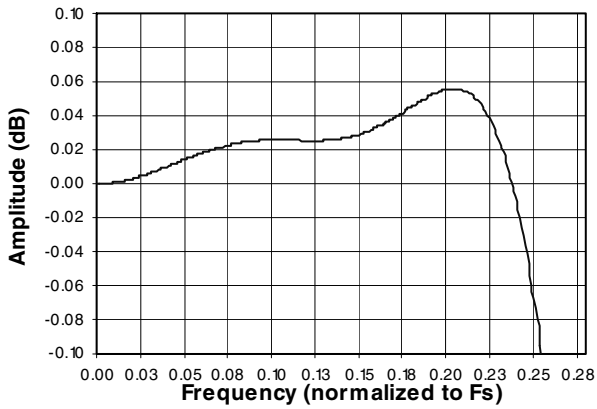


Figure 44. ADC Quad Speed Passband Ripple

Release	Date	Changes
A1	May 2004	Initial Advance Release.
PP1	August 2004	Preliminary Release. – Updated the VA power-down mode supply current specification on page 19.

Table 18. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com